SMIC 0.18 μm
I/O Cell Library (*SP018W*)
Data Book

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Semiconductor Manufacturing International Corporation

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Document Revision History

VERSION	*EFFECTIVE DATE*	*NOTE AND CHANGE DESCRIPTION*
0.1	2 April 2003	Initial version of data book
1.0	30 June 2003	● DC specification: R_{PU}, R_{PD}, V_{T+}, V_{T-}, I_{OL} & I_{OH} (2, 4, 8, 12, 16 and 24mA) ● Appendix A (Maximum Allowable Current) ● Update design tools
1.1	9 October 2003	● Upgrade Appendix A (Maximum Allowable Current) ● Digital power and ground cells description
1.2	7 November 2003	● Describe FP pin in I/O Layout Configuration section ● Update design tools ● PCI cell description in detail ● Appendix B: Maximum Allowable Current for Analog power and ground cells
1.3	1 December 2003	● Description of IP usage statement on page iii ● Add new analog power/ground cells in cell categories ● Appendix A and B
1.4	23 August 2004	● Add three cells: PANA3APW, PVDD1ANPW, PVSS1ANPW ● Update description of analog cells ● Add one Characterization Condition in Chapter 5 ● Update Appendix A and B
1.5	February 28, 2005	● Add tie-high/tie-low description in chapter 4 ● Modify description of power cells in chapter 6

TABLE OF CONTENTS

1. Introduction

This data book provides general technical information and property of SMIC 0.18μm logic I/O Library (*SP018W*). All I/O pads are matched with the design requirement of SMIC 0.18μm Logic 1P6M Salicide 1.8V/3.3V Design Rules (TD-L018-DR-2001). Table 1 describes the process and physical specification of the Library. It should be noted that *SP018W* support design with four, five or six layers of metal applications. I/O application criteria are listed as shown in Table 2.

Table 1 Physical Specification

Items	Contents
Process	SMIC 0.18μm Logic 1P6M Salicide 1.8V/3.3V Process
Metal Layers	Suitable for 4,5 and 6 layers application
Cell Size (Width * height)	76 um * 210 um including pads

Table 2 I/O application table

I/O Type	Option and possible Combination
Standard I/O interface pads	3V/5V input tolerance, 3.3V output Schmitt trigger input LVCMOS / LVTTL level Tri-State Slew rate controlled (Low noise) Pull-Up Tr. Resistor Range: 39-116 (K ohm) Pull-Down Tr. Resistor Range: 40-108(K ohm) 2, 4, 8,12, 16, 24mA driving strength per I/O pads
High Drive clock buffer	**(NOT Ready YET)** Pad in core out, core in core out
Crystal I/O pads	Different frequencies
Special I/O pads	PCI (3.3V, 33/66MHz)

1.1. Outline Of the Document

The materials in this data book also covered the **Design Tools Support**, **I/O Layout Configuration**, **Cell Categories, DC and AC Specification** about SMIC *SP018W* I/O Library and **Data Sheet** that contain the cell information and characteristics of each I/O pad in the Library.

2. Design Tools Support

SMIC I/O library (*SP018W*) design views support the following popular industry design tools:

Front end

- Verilog models
- VHDL models
- Synopsys synthesis models
- Cadence place-and route
- Synopsys place-and route

Back end

- GDSII
- LVS Netlist

SP018W I/O library models will comply with the following file formats and versions. The CAD tools and version that are used and supported the *SP018W* I/O library design flow are also listed in Table 3.

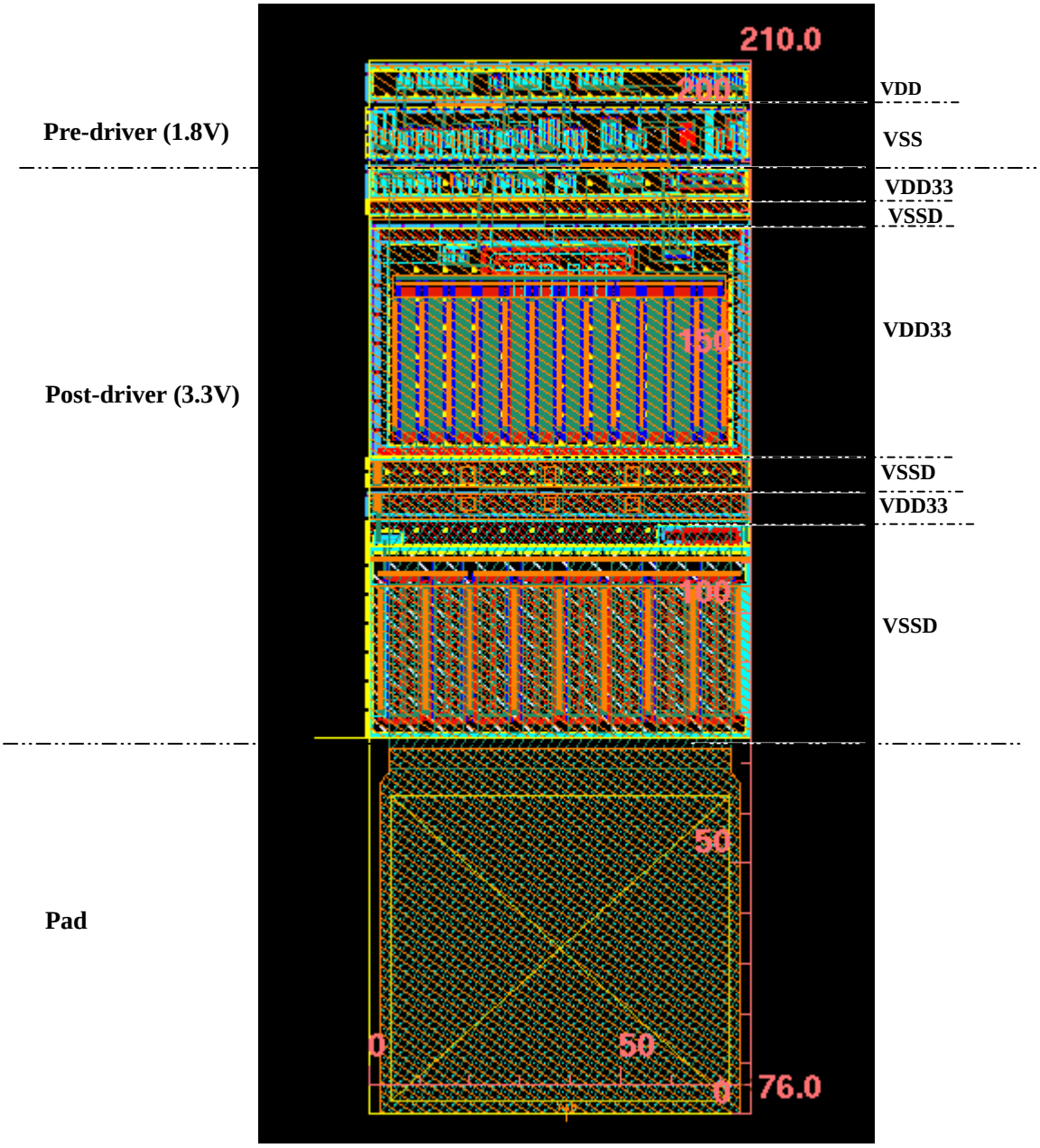
Table 3. Design tools facility

Design Phase	Tool and Vendor	Tool Version	Files Format
Verilog Simulation	NC-Verilog (Cadence)	2003. 4	.v
	Verilog-XL (Cadence)	3.40.S002	.v
	VCS (Synopsys)	6.2R16	.v
VHDL/Vital Simulation	NC-VHDL (Cadence)	3.4	.vhd
Synthesis	Design Compiler (Synopsys)	2003.06	.lib, .slib, .db, .sdb
	Physical Compiler (Synopsys)	2003.06	.plib, .pdb
	BuildGates/PKS (Cadence)	5.09-s043+2	.tlf
Static timing / Delay calculation	PrimeTime (Synopsys)	2002.09-SP1	.lib, .db
	Pearl (Cadence)	5.1-s068	.tlf
	Design Compiler (Synopsys)	2003.06	.lib, .db
Schematic simulation	Avant! HSPICE	2002.2.2	.sp
	Eldo (Mentor)	V6.2_1.1	.cir
Power Estimation/Optimum	Power Compiler (Synopsys)	2003.06	.lib, .db
Place-and Route	Silicon Ensemble (Cadence)	5.4	
	Apollo-II (Avant!)	U2003.03	
Back end Verification (DRC and LVS)	Layout: Virtuoso (Cadence)	V5.0.0	GDSII
	Layout: Laker (Silicon Canvas, Inc.)	V2.3	
	Layout: Mentor: IC Station	8.9_11.1	

	DRC: Dracula(Cadence);	Rev.1.2	
	Hercules (Avant!)	Rev.1.3	
	Calibre(Mentor)	V9.3_4.7	CDL netlist
	LVS: Dracula (Cadence);	4.9.03-2003	
	Hercules (Avant!)	U-2003.03.0052	
	Calibre(Mentor)	V9.3_4.7	

3. I/O Layout Configuration

In this section I/O layout sample, the detail of the I/O layout configuration and structure of power supplies are presented. SMIC I/O structure is constructed by pre-driver and post-driver section as shown in the layout sample below. Each section has its own function. Pre-driver provides logic operation for I/O circuit, and post-driver provides large driving capability and ESD protection ability.



The pre-driver section contains VDD and VSS ports. In which VDD is connecting to the 1.8V power ring of pre-driver and VSS is connecting to the ground of pre-driver respectively.
The post-driver section contains various ports and their functions are Connecting to the 3.3V power and ground ring of post-driver, and connecting to various guard ring for latch-up and ESD protection purposes.

Note that SMIC *SP018W* I/O uses both 1.8V (VDD) and 3.3V (VDD33) power supplies to adept its 1.8V input of core logic and 3.3V output signal with 5V tolerant. 5V tolerant means maximum supply voltage can be handled by the I/O is up to 5V. For noise immunity consideration, ground power supplies separated into two parts where VSS for pre-driver section and VSSD for post-driver section.
FP stands for 'From Power Pad' and FP pin is for global signal. Under normal condition, FP is activated by PVDD2W to 'HIGH' (3.3V). FP rail will be automatically connected while joining with other digital I/O cells.

4. Cell Categories

Cell categories of digital and analog I/O cells and their functions description are listed in Table 4. The suffix of cell means the drive strength and x can be 2, 4, 8, 12, 16 and 24. For examples, PB2W means the drive strength is 2mA and PB24W mean the drive strength is 24mA.

Note: When cell pin is needed to connect power/ground, in order to improve ESD performance, the user must use one tie-high/tie-low cell to tie the IO cell pin to power/ground by using tie-high/tie-low cells of user's standard cell library. Please refer to application note for more information about tie-high/tie-low.

Table 4. Cell categories

Cells Name	Function Description of Digital I/O Cells
PIDW	Input pad with pull down
PISDW	Schmitt trigger input pad with pull down
PICDW	Input pad with enable controlled pull down
PIW	Input pad
PISW	Schmitt trigger input pad
PIUW	Input pad with pull-up
PISUW	Schmitt trigger input pad with pull-up
PICUW	Input pad with enable controlled pull-up
PXWE1W	Crystal oscillator with high enable
PXWE2W	Crystal oscillator with high enable
PXWE3W	Crystal oscillator with high enable
PX1W	Crystal oscillator
PX2W	Crystal oscillator
PX3W	Crystal oscillator
PVDD1W	Vdd power pad for I/O pre-driver & core
PVDD2W	Vdd power pad for I/O post-driver
PVSS1W	Vss ground pad for I/O pre-driver & core
PVSS2W	Vss ground pad for I/O post-driver
PVSS3W	Vss ground pad for ALL (I/O pre-driver, post-driver & core)

SMIC PCI is complies with PCI Local Bus Specification, Revision 2.2. PCI3BWhas same functionality as PCI6BW however PCI3BWwill consume more power and slower than PCI6BW In addition, please note that, a 66 MHz PCI device operates as a 33MHz PCI device when it is

connected to a 33MHz PCI bus. Similarly, if any 33 MHz PCI devices are connected to a 66 MHz PCI bus, the 66 MHz PCI bus will operate as a 33 MHz PCI bus. Thus right choice of PCI pads is totally depend on user's specific implement.

Cells Name	Function Description of Digital Bi-input I/O Cells
PCI3BW	3-state, output 33Mhz,pci buffer pad with input and limited slew rate
PCI3BSW	3-state, output 33Mhz,pci buffer pad with Schmitt trigger input and limited slew rate
PCI6BW	3-state, output 66Mhz,pci buffer pad with input and limited slew rate
PCI6BSW	3-state, output 66Mhz,pci buffer pad with Schmitt trigger input and limited slew rate
PB2W	CMOS 3-state output pad with input
PB4W	CMOS 3-state output pad with input
PB8W	CMOS 3-state output pad with input
PB12W	CMOS 3-state output pad with input
PB16W	CMOS 3-state output pad with input
PB24W	CMOS 3-state output pad with input
PBS2W	CMOS 3-state output pad with Schmitt trigger input
PBS4W	CMOS 3-state output pad with Schmitt trigger input
PBS8W	CMOS 3-state output pad with Schmitt trigger input
PBS12W	CMOS 3-state output pad with Schmitt trigger input
PBS16W	CMOS 3-state output pad with Schmitt trigger input
PBS24W	CMOS 3-state output pad with Schmitt trigger input
PBCD2W	3-state output pad with input and enable controlled pull down
PBCD4W	3-state output pad with input and enable controlled pull down
PBCD8W	3-state output pad with input and enable controlled pull down
PBCD12W	3-state output pad with input and enable controlled pull down
PBCD16W	3-state output pad with input and enable controlled pull down
PBCD24W	3-state output pad with input and enable controlled pull down
PBD2W	CMOS 3-state output pad with input and pull down
PBD4W	CMOS 3-state output pad with input and pull down
PBD8W	CMOS 3-state output pad with input and pull down
PBD12W	CMOS 3-state output pad with input and pull down
PBD16W	CMOS 3-state output pad with input and pull down
PBD24W	CMOS 3-state output pad with input and pull down
PBSD2W	CMOS 3-state output pad with Schmitt trigger input and pull down
PBSD4W	CMOS 3-state output pad with Schmitt trigger input and pull down

PBSD8W	CMOS 3-state output pad with Schmitt trigger input and pull down
PBSD12W	CMOS 3-state output pad with Schmitt trigger input and pull down
PBSD16W	CMOS 3-state output pad with Schmitt trigger input and pull down
PBSD24W	CMOS 3-state output pad with Schmitt trigger input and pull down
PO2W	CMOS output pad
PO4W	CMOS output pad
PO8W	CMOS output pad
PO12W	CMOS output pad
PO16W	CMOS output pad
PO24W	CMOS output pad
POT2W	CMOS 3-state output pad
POT4W	CMOS 3-state output pad
POT8W	CMOS 3-state output pad
POT12W	CMOS 3-state output pad
POT16W	CMOS 3-state output pad
POT24W	CMOS 3-state output pad
PBCU2W	3-state output pad with input and enable controlled pull-up
PBCU4W	3-state output pad with input and enable controlled pull-up
PBCU8W	3-state output pad with input and enable controlled pull-up
PBCU12W	3-state output pad with input and enable controlled pull-up
PBCU16W	3-state output pad with input and enable controlled pull-up
PBCU24W	3-state output pad with input and enable controlled pull-up
PBU2W	CMOS 3-state output pad with input and pull-up
PBU4W	CMOS 3-state output pad with input and pull-up
PBU8W	CMOS 3-state output pad with input and pull-up
PBU12W	CMOS 3-state output pad with input and pull-up
PBU16W	CMOS 3-state output pad with input and pull-up
PBU24W	CMOS 3-state output pad with input and pull-up
PBSU2W	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU4W	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU8W	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU12W	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU16W	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBSU24W	CMOS 3-state output pad with Schmitt trigger input and pull-up
PBL8W	CMOS 3-state output pad with input and limited slew rate
PBL12W	CMOS 3-state output pad with input and limited slew rate
PBL16W	CMOS 3-state output pad with input and limited slew rate
PBL24W	CMOS 3-state output pad with input and limited slew rate
PBSL8W	CMOS 3-state output pad with Schmitt trigger input and limited slew rate
PBSL12W	CMOS 3-state output pad with Schmitt trigger input and limited slew rate

PBSL16W	CMOS 3-state output pad with Schmitt trigger input and limited slew rate
PBSL24W	CMOS 3-state output pad with Schmitt trigger input and limited slew rate
PBCDL8W	3-state output pad with input, limited slew rate and enable controlled pull down
PBCDL12W	3-state output pad with input, limited slew rate and enable controlled pull down
PBCDL16W	3-state output pad with input, limited slew rate and enable controlled pull down
PBCDL24W	3-state output pad with input ,limited slew rate and enable controlled pull down
PBDL8W	CMOS 3-state output pad with input, pull down, and limited slew rate
PBDL12W	CMOS 3-state output pad with input, pull down, and limited slew rate
PBDL16W	CMOS 3-state output pad with input, pull down, and limited slew rate
PBDL24W	CMOS 3-state output pad with input, pull down, and limited slew rate
PBSDL8W	CMOS 3-state output pad with Schmitt trigger input, pull down, and limited slew rate
PBSDL12W	CMOS 3-state output pad with Schmitt trigger input, pull down, and limited slew rate
PBSDL16W	CMOS 3-state output pad with Schmitt trigger input, pull down, and limited slew rate
PBSDL24W	CMOS 3-state output pad with Schmitt trigger input, pull down, and limited slew rate
POL8W	CMOS output pad with limited slew rate
POL12W	CMOS output pad with limited slew rate
POL16W	CMOS output pad with limited slew rate
POL24W	CMOS output pad with limited slew rate
POTL8W	CMOS 3-state output pad with limited slew rate
POTL12W	CMOS 3-state output pad with limited slew rate
POTL16W	CMOS 3-state output pad with limited slew rate
POTL24W	CMOS 3-state output pad with limited slew rate
PBCUL8W	3-state output pad with input, limited slew rate and enable controlled pull-up
PBCUL12W	3-state output pad with input, limited slew rate and enable controlled pull-up
PBCUL16W	3-state output pad with input, limited slew rate and enable controlled pull-up
PBCUL24W	3-state output pad with input, limited slew rate and enable controlled pull-up
PBUL8W	CMOS 3-state output pad with input, pull-up, and limited slew rate

PBUL12W	CMOS 3-state output pad with input, pull-up, and limited slew rate
PBUL16W	CMOS 3-state output pad with input, pull-up, and limited slew rate
PBUL24W	CMOS 3-state output pad with input, pull-up, and limited slew rate
PBSUL8W	CMOS 3-state output pad with Schmitt trigger input, pull-up, and limited slew rate
PBSUL12W	CMOS 3-state output pad with Schmitt trigger input, pull-up, and limited slew rate
PBSUL16W	CMOS 3-state output pad with Schmitt trigger input, pull-up, and limited slew rate
PBSUL24W	CMOS 3-state output pad with Schmitt trigger input, pull-up, and limited slew rate

Note: **SMIC does not recommend customers to use this library to interface with non-SMIC analog macros. Misuse of the analog library may cause damages to customer's product.**

Cells Name	Function Description of Analog I/O Cells**
PANA2APW	Analog IO pad used with power-cut cell for high frequency application
PANA2AP1W	Similar to PANA2APW but utilizes a different post-driver power
PANA1APW	Analog IO pad used with power-cut cell for low frequency application
PANA1AP1W	Similar to PANA1APW but utilizes a different post-driver power
PDIODEW	Power-Cut Cell for same voltage level between digital and analog
PDIODE8W	Power-Cut Cell for High Voltage Drop for difference voltage level between digital and analog
PVDD3APW	VDD analog PAD
PVSS3APW	VSS analog PAD
PVDD1APW	VDD analog PAD
PVSS1APW	VSS analog PAD
PVDD5APW	VDD analog PAD
PVSS5APW	VSS analog PAD
PVDD1AP1W	VDD analog PAD
PVSS1AP1W	VSS analog PAD
PVDD4APW	VDD analog PAD

PVSS4APW	VSS analog PAD
PVDD2APW	VDD analog PAD
PVSS2APW	VSS analog PAD
PVDD1CAPW	VDD analog PAD (for 1.8v)
PVDD1CAP1W	VDD analog PAD (for 1.8v)
PVSS1CAPW	VSS analog PAD (for 1.8v)
PVSS1CAP1W	VSS analog PAD (for 1.8v)
PVSS3CAPW	VSS analog PAD (for 1.8v)
PVDD3CAPW	VDD analog PAD (for 1.8v)
PANA4APW	Analog IO pad used with power-cut cell for high frequency application and higher maximum allowable current capability
PANA3APW	Analog IO pad used with power-cut cell for high frequency application and 5V tolerance
PVDD1ANPW	VDD analog PAD within digital power domain
PVSS1ANPW	VSS analog PAD within digital power domain

**Please refer to application note for more information.

Cells Name	Function Description of Filler Cells
PCORNERW	Corner cell
PFILL001W	Filler cell
PFILL01W	Filler cell
PFILL1W	Filler cell
PFILL10W	Filler cell
PFILL2W	Filler cell
PFILL20W	Filler cell
PFILL22W	Filler cell
PFILL5W	Filler cell
PFILL50W	Filler cell
PFILL001AW	Filler cell for analog IO cells
PFILL01AW	Filler cell for analog IO cells
PFILL10AW	Filler cell for analog IO cells
PFILL1AW	Filler cell for analog IO cells
PFILL20AW	Filler cell for analog IO cells
PFILL2AW	Filler cell for analog IO cells
PFILL50AW	Filler cell for analog IO cells
PFILL5AW	Filler cell for analog IO cells

5. DC and AC Specification

This section provided DC and AC information of I/O library. It includes recommended operating conditions and the absolute maximum rating conditions for the I/O library. The device should be operated under recommended operating condition. Since, absolute maximum rating condition can either caused device reliability problem or damage the device sufficiently to cause immediate failure. ESD of *SP018W* library meets HBM-2KV and MM-200V.

5.1 DC Specifications

The I/O library is LVTTL/LVCMOS compatible, recommended DC operating conditions and electrical characteristics are listed in Table 5. The Absolute Maximum Ratings Condition is shown in Table 6.

Table 5. Recommended Operating Conditions

Symbol	Parameter		Min.	Norm	Max
VDD	Pre-driver supply voltage		1.62V	1.8V	1.98V
VDD33	I/O supply voltage		2.97V	3.3V	3.63V
V_{IH}	Input High Voltage		2.0V		5.5V
V_{IL}	Input Low Voltage		-0.3V		0.8V
V_T	Threshold point		1.45V	1.58V	1.74V
V_{T+}	Schmitt trig Low to High threshold point		1.44V	1.50V	1.56V
V_{T-}	Schmitt trig. High to Low threshold point		0.89V	0.94V	0.99V
T_J	Junction Temperature		0 ℃	25℃	125℃
I_L	Input Leakage Current				±10uA
I_{OZ}	Tri-State output leakage current				±10uA
R_{PU}	Pull-up Resistor		39kohm	65kohm	116kohm
R_{PD}	Pull-down Resistor		40kohm	56kohm	108kohm
V_{OL}	Output low voltage @I_{OL}=2,4…24mA				0.4V
V_{OH}	Output high voltage @ I_{OH}=2,4…24mA		2.4V		
I_{OL}	Low level output current @V_{OL}=0.4V	2mA	2.4mA	4.0mA	5.0mA
		4mA	4.7mA	8.0mA	10mA
		8mA	9.4 mA	15.9mA	19.8mA
		12mA	14.2mA	23.9mA	29.8mA
		16mA	18.9mA	31.8mA	39.8mA
		24mA	28.3mA	47.8mA	59.7mA
I_{OH}	High level output current @VOH=2.4V	2mA	2.8 mA	5.9mA	9.5mA
		4mA	5.6mA	11.9mA	19mA
		8mA	11.2mA	23.8mA	38.3mA

	12mA	16.8mA	35.7mA	57 mA
	16mA	22 mA	47.7mA	76mA
	24mA	33.7mA	71.5mA	115mA

Table 6. Absolute Maximum Ratings

Parameters	Value
Input Voltage, VI	-0.5v~6v
Output Voltage, Vo	-0.5v~4.6v
Pre-driver power supply voltage	-0.5v~2.5v
Post-driver Power supply voltage	-0.5v~4.6v
Operation Temperature, T_{OPT}	-40℃~ +125℃
Storage Temperature, T_{STG}	-65℃~ +150℃

5.2 AC Specifications

AC specifications are characterized in four operating condition. Those are worst-case, typical-case, best-case and low temperature conditions. The detail of each condition is listed in the Table 7.

Table 7. AC Characterization Condition

Type	Condition
Typical case	VDD33=3.3V, VDD=1.8V temperature=25℃ Process = Typical-Typical
Best case	VDD33=3.63V, VDD=1.98V temperature=0℃ Process = Fast-Fast
Worst case	VDD33=2.97V, VDD=1.62V temperature=125℃ Process =Slow-Slow
Low temperature	VDD33=3.63V, VDD=1.98V temperature=-40℃ Process = Fast-Fast

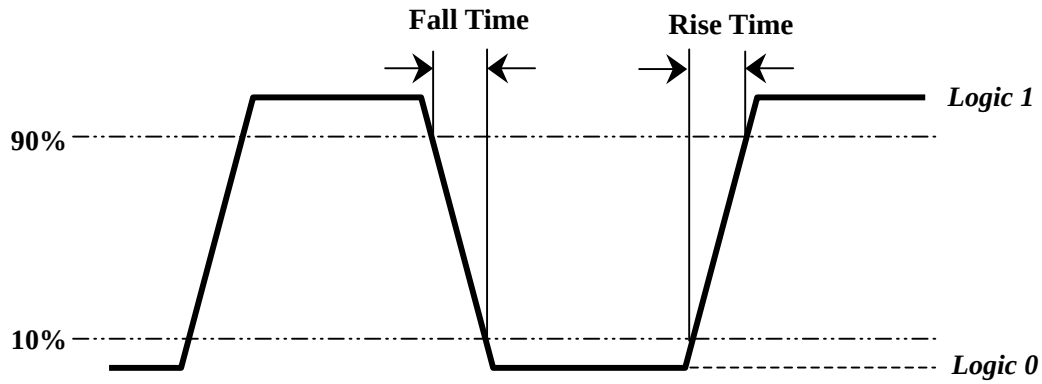
5.3 Timing Parameters

The timing parameters that are used in cell characterization are transition time (Rise/Fall) and Propagation time delay. These two important parameters are addressed in the next section.

Transition Time (Rise/Fall)

The rise time is defined as the transition time from output logic low to logic high. Conversely, the fall time, also defined as the transition time from output logic high to output logic low. This transition time is measured at specified percentages (10% ~ 90%) of the output waveform amplitude (refer to Figure 1).

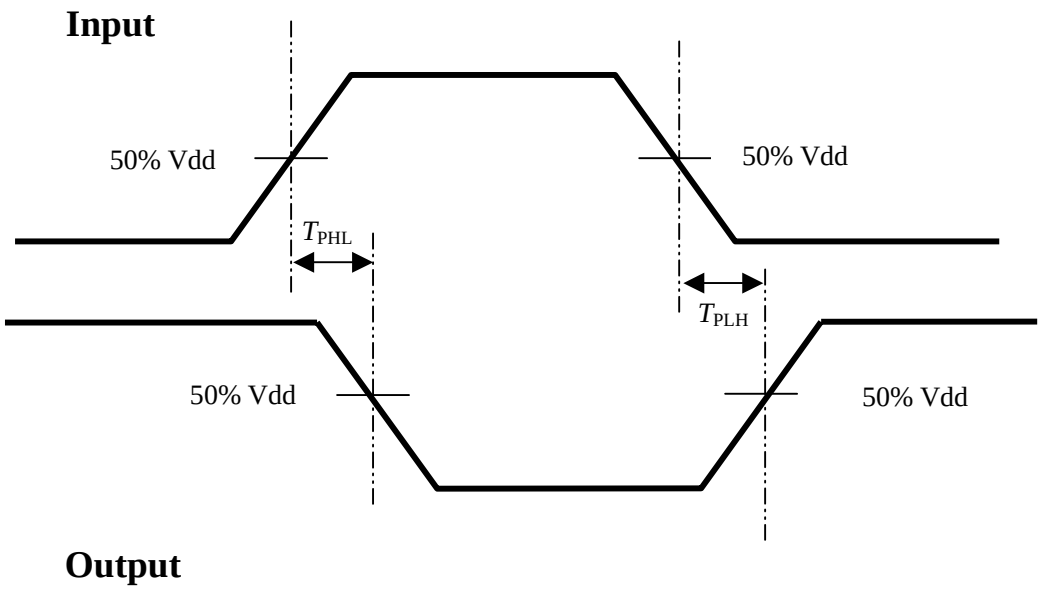
Figure 1. Rise/Fall Transition Time



Propagation Delays

Propagation delays are time delays inherent in all switching circuits. It is the minimum time required for data to be propagated from the input of the cell to the output. The propagation delay time T_{PHL} and T_{PLH} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively. By definition, it is the time from the point where the input transition reaches 50% of the supply voltage to the point where the output transition reaches 50% of the supply voltage (Refer to Figure 2). If the input triggers the rising output, the propagation delay is referred to as a rising delay (T_{PLH}). If the input triggers the falling output, the delay is referred to as a falling delay (T_{PHL}).

Figure 2. Propagation delay of data signal at input/output of the cell



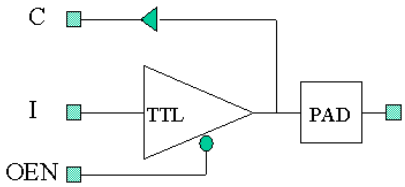
6. Data Sheet

Notice: Pin Capacitance values are NOT READY YET

PCI3BW

PCI3BW

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH INPUT AND LIMITED SLEW RATE, 5V-Tolerant



● Truth Table

Input		Output	
OEN	**I**	**PAD**	**C**
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PCI3BW	**1**	**384**

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PCI3BW				

PCI3BW

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH
INPUT AND LIMITED SLEW RATE, 5V-Tolerant

● Propagation Delay(ns)

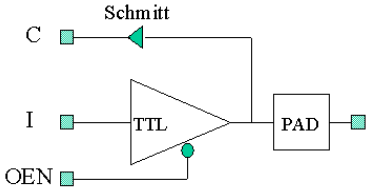
VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PCI3BW	I->PAD (fall)	1.965	2.454	2.866	4.241	0.0196*Cload+1.828
PCI3BW	I->PAD (rise)	1.854	2.319	2.715	4.089	0.0193*Cload+1.7068
PCI3BW	OEN->PAD (fall)	1.413	2.091	2.59	4.101	0.0230*Cload+1.3125
PCI3BW	OEN->PAD (rise)	1.385	1.989	2.448	3.934	0.022*Cload+1.2565

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PCI3BW	PAD->C (fall)	0.2653	0.2687	0.2749	0.288	0.2360*Cload+0.2659
PCI3BW	PAD->C (rise)	0.2549	0.257	0.2614	0.2714	0.1731*Cload+0.2551

PCI3BSW

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH
INPUT AND LIMITED SLEW RATE, 5V-Tolerant



● Truth Table

Input			Output
OEN	**I**	**PAD**	**C**
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PCI3BSW	**1**	**392.6**

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PCI3BSW				

PCI3BSW

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH INPUT AND LIMITED SLEW RATE, 5V-Tolerant

● Propagation Delay(ns)

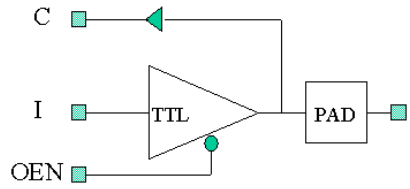
VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PCI3BSW	I->PAD (fall)	1.964	2.454	2.866	4.241	0.0196*Cload+1.8277
PCI3BSW	I->PAD (rise)	1.853	2.318	2.714	4.088	0.0193*Cload+1.7058
PCI3BSW	OEN->PAD (fall)	1.412	2.09	2.589	4.101	0.0230*Cload+1.3117
PCI3BSW	OEN->PAD (rise)	1.384	1.988	2.447	3.933	0.022*Cload+1.2555

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PCI3BSW	PAD->C (fall)	0.4542	0.4565	0.4613	0.4722	0.1888*Cload+0.4544
PCI3BSW	PAD->C (rise)	0.4199	0.4226	0.4275	0.4349	0.1444*Cload+0.4211

PCI6BW

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH INPUT AND LIMITED SLEW RATE, 5V-Tolerant



● Truth Table

Input			Output
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PCI6BW	1	303

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD

PCI6BW

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH
INPUT AND LIMITED SLEW RATE, 5V-Tolerant

● Propagation Delay(ns)

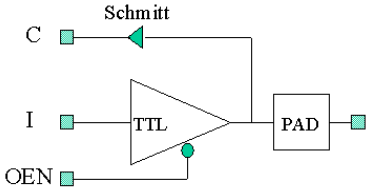
VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PCI6BW	I->PAD (fall)	1.641	2.127	2.538	3.95	0.0199*Cload+1.4943
PCI6BW	I->PAD (rise)	1.532	1.959	2.332	3.66	0.0184*Cload+1.3817
PCI6BW	OEN->PAD (fall)	1.348	1.97	2.434	3.895	0.0219*Cload+1.2346
PCI6BW	OEN->PAD (rise)	1.23	1.719	2.129	3.542	0.0200*Cload+1.08

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PCI6BW	PAD->C (fall)	0.2653	0.2687	0.2749	0.288	0.2360*Cload+0.2659
PCI6BW	PAD->C (rise)	0.2549	0.257	0.2614	0.2714	0.1731*Cload+0.2551

PCI6BSW

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH
INPUT AND LIMITED SLEW RATE, 5V-Tolerant



● Truth Table

Input			Output
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PCI6BSW	1	300.3

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PCI6BSW				

PCI6BSW

3-STATE OUTPUT 33MHz PCI BUFFER PAD WITH INPUT AND LIMITED SLEW RATE, 5V-Tolerant

● Propagation Delay(ns)

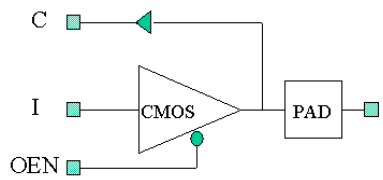
VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PCI6BSW	I->PAD (fall)	1.641	2.127	2.538	3.95	0.0199*Cload+1.4943
PCI6BSW	I->PAD (rise)	1.531	1.958	2.331	3.659	0.0184*Cload+1.3807
PCI6BSW	OEN->PAD (fall)	1.347	1.969	2.433	3.895	0.0219*Cload+1.2338
PCI6BSW	OEN->PAD (rise)	1.229	1.718	2.128	3.541	0.0200*Cload+1.079

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PCI6BSW	PAD->C (fall)	0.4542	0.4565	0.4613	0.4722	0.1888*Cload+0.4544
PCI6BSW	PAD->C (rise)	0.4199	0.4226	0.4275	0.4349	0.1444*Cload+0.4211

PBxW

CMOS 3-STATE OUTPUT PAD WITH INPUT, 5V-Tolerant



● Truth Table

Input		Output	
OEN	**I**	**PAD**	**C**
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PB2W	1	83.7
PB4W	1	96.72
PB8W	1	97.99
PB12W	1	110.6
PB16W	1	107.2
PB24W	1	121.7

Note: The suffix of cell means its drive strength, for examples, PB2 means the drive strength is 2mA and PB24 means the drive strength is 24mA.

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PB2W				
PB4W				
PB8W				
PB12W				
PB16W				
PB24W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB2W	PAD->C (fall)	0.2888	0.2944	0.297	0.3081	0.2389*Cload+0.2887
PB2W	PAD->C (rise)	0.3392	0.3452	0.3515	0.3593	0.1974*Cload+0.3419
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB2W	I->PAD (fall)	2.988	6.618	10.22	23.59	0.1789*Cload+1.2381
PB2W	I->PAD (rise)	2.947	6.632	10.26	23.79	0.1812*Cload+1.1677
PB2W	OEN->PAD (fall)	2.824	6.454	10.05	23.42	0.1789*Cload+1.0711
PB2W	OEN->PAD (rise)	2.969	6.625	10.25	23.77	0.1808*Cload+1.1855

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB4W	PAD->C (fall)	0.2878	0.2933	0.296	0.3071	0.2374*Cload+0.2877
PB4W	PAD->C (rise)	0.3392	0.3452	0.3515	0.3593	0.1974*Cload+0.3419
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB4W	I->PAD (fall)	1.822	3.63	5.427	12.13	0.0895*Cload+0.9416
PB4w	I->PAD (rise)	1.744	3.597	5.427	12.22	0.0910*Cload+0.8557
PB4W	OEN->PAD (fall)	1.727	3.535	5.332	12.04	0.0896*Cload+0.8425
PB4W	OEN->PAD (rise)	1.774	3.613	5.432	12.21	0.0907*Cload+0.8821

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB8W	PAD->C (fall)	0.288	0.2936	0.2961	0.3073	0.2403*Cload+0.2878
PB8W	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB8W	I->PAD (fall)	1.288	2.197	3.093	6.444	0.0448*Cload+0.8475
PB8W	I->PAD (rise)	1.227	2.16	3.079	6.491	0.0457*Cload+0.7828
PB8W	OEN->PAD (fall)	1.239	2.144	3.041	6.391	0.0447*Cload+0.8011
PB8W	OEN->PAD (rise)	1.254	2.182	3.096	6.497	0.0455*Cload+0.8116

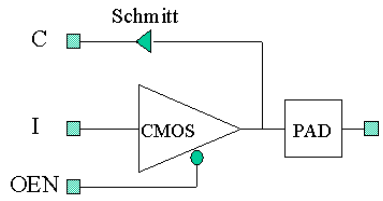
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB12W	PAD->C (fall)	0.2878	0.2933	0.296	0.3071	0.2374*Cload+0.2877
PB12W	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB12W	I->PAD (fall)	1.131	1.74	2.338	4.571	0.0299*Cload+0.8378
PB12W	I->PAD (rise)	1.085	1.718	2.333	4.613	0.0306*Cload+0.7925
PB12W	OEN->PAD (fall)	1.097	1.701	2.299	4.53	0.0298*Cload+0.805
PB12W	OEN->PAD (rise)	1.106	1.735	2.348	4.621	0.0305*Cload+0.8131

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB16W	PAD->C (fall)	0.288	0.2936	0.2961	0.3073	0.2403*Cload+0.2878
PB16W	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB16W	I->PAD (fall)	1.071	1.527	1.977	3.652	0.0224*Cload+0.8527
PB16W	I->PAD (rise)	1.035	1.525	1.991	3.704	0.0231*Cload+0.8221
PB16W	OEN->PAD (fall)	1.041	1.496	1.944	3.618	0.0224*Cload+0.8207
PB16W	OEN->PAD (rise)	1.053	1.54	2.003	3.712	0.0231*Cload+0.8353

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PB24W	PAD->C (fall)	0.288	0.2906	0.2966	0.3099	0.2274*Cload+0.2883
PB24W	PAD->C (rise)	0.3399	0.3422	0.3464	0.3554	0.1616*Cload+0.3403
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PB24W	I->PAD (fall)	1.131	1.45	1.752	2.87	0.0151*Cload+0.9891
PB24W	I->PAD (rise)	1.094	1.453	1.774	2.925	0.0158*Cload+0.9622
PB24W	OEN->PAD (fall)	1.107	1.425	1.727	2.843	0.0150*Cload+0.9692
PB24W	OEN->PAD (rise)	1.1	1.456	1.775	2.923	0.0158*Cload+0.9642

PBSxW

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT , 5V-Toleran



● Truth Table

Input			Output
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBS2W	1	80.56
PBS4W	1	89.9
PBS8W	1	95.26
PBS12W	1	97.35
PBS16W	1	97.35
PBS24W	1	123.6

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBS2W				
PBS4W				
PBS8W				
PBS12W				
PBS16W				
PBS24W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS2W	PAD->C (fall)	0.4483	0.451	0.4571	0.4704	0.2288*Cload+0.4487
PBS2W	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS2W	I->PAD (fall)	2.985	6.615	10.21	23.58	0.1789*Cload+1.2316
PBS2W	I->PAD (rise)	2.942	6.626	10.26	23.79	0.1812*Cload+1.165
PBS2W	OEN->PAD (fall)	2.821	6.451	10.05	23.42	0.1789*Cload+1.0696
PBS2W	OEN->PAD (rise)	2.965	6.619	10.24	23.77	0.1808*Cload+1.1805

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS4W	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636	0.1487*Cload+0.4480
PBS4W	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS4W	I->PAD (fall)	1.82	3.629	5.426	12.13	0.0896*Cload+0.9352
PBS4W	I->PAD (rise)	1.743	3.595	5.424	12.22	0.0910*Cload+0.8542

PBS4W	OEN->PAD (fall)	1.726	3.533	5.33	12.03	0.0895*Cload+0.8441
PBS4W	OEN->PAD (rise)	1.772	3.61	5.43	12.21	0.0907*Cload+0.8803

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS8W	PAD->C (fall)	0.4508	0.4531	0.4578	0.4685	0.1859*Cload+0.4510
PBS8W	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS8W	I->PAD (fall)	1.287	2.196	3.093	6.443	0.0448*Cload+0.8467
PBS8W	I->PAD (rise)	1.226	2.159	3.078	6.49	0.0457*Cload+0.7818
PBS8W	OEN->PAD (fall)	1.238	2.144	3.04	6.39	0.0448*Cload+0.795
PBS8W	OEN->PAD (rise)	1.253	2.181	3.095	6.496	0.0455*Cload+0.8106

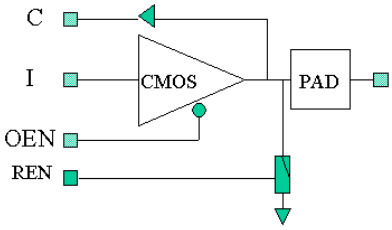
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS12W	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636	0.1487*Cload+0.4480
PBS12W	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS12W	I->PAD (fall)	1.13	1.739	2.338	4.57	0.0299*Cload+0.8371
PBS12W	I->PAD (rise)	1.084	1.717	2.332	4.612	0.0306*Cload+0.7915
PBS12W	OEN->PAD (fall)	1.096	1.7	2.298	4.53	0.0298*Cload+0.8042
PBS12W	OEN->PAD (rise)	1.105	1.735	2.348	4.621	0.0305*Cload+0.8128

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS16	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636	0.1487*Cload+0.4480
PBS16	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS16W	I->PAD (fall)	1.13	1.739	2.338	4.57	0.0299*Cload+0.8371
PBS16W	I->PAD (rise)	1.084	1.717	2.332	4.612	0.0306*Cload+0.7915
PBS16W	OEN->PAD (fall)	1.096	1.7	2.298	4.53	0.0298*Cload+0.8042
PBS16W	OEN->PAD (rise)	1.105	1.735	2.348	4.621	0.0305*Cload+0.8128

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBS24W	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636	0.1487*Cload+0.4480
PBS24W	PAD->C (rise)	0.4931	0.4953	0.5001	0.5119	0.2002*Cload+0.4931
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBS24W	I->PAD (fall)	1.131	1.45	1.752	2.87	0.0151*Cload+0.9891
PBS24W	I->PAD (rise)	1.094	1.453	1.773	2.925	0.0159*Cload+0.9566
PBS24W	OEN->PAD (fall)	1.107	1.425	1.726	2.843	0.0151*Cload+0.9636
PBS24W	OEN->PAD (rise)	1.099	1.456	1.775	2.923	0.0158*Cload+0.964

PBCDxW

CMOS 3-STATE OUTPUT PAD WITH INPUT and CONTROLLABLE PULLDOWN, 5V-Tolerant



● Truth Table

Input			Output	
REN	**OEN**	**I**	**PAD**	**C**
x	1	x	0	0
x	1	x	1	1
0	1	x	pull-down	0
1	1	x	Z	x
x	0	0	0	0
x	0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PBCD2W	**1**	**75.88**
PBCD4W	**1**	**89.59**
PBCD8W	**1**	**96.57**
PBCD12W	**1**	**103.3**
PBCD16W	**1**	**106.6**

PBCD24W	**1**	**122.6**

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBCD2W				
PBCD4W				
PBCD8W				
PBCD12W				
PBCD16W				
PBCD24W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCD2W	PAD->C (fall)	0.2885	0.2939	0.2968	0.3078	0.2346*Cload+0.2885
PBCD2W	PAD->C (rise)	0.3432	0.3456	0.3511	0.3596	0.1559*Cload+0.3444

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCD2W	I->PAD (fall)	2.988	6.618	10.22	23.59	0.1789*Cload+1.2381
PBCD2W	I->PAD (rise)	2.947	6.632	10.26	23.79	0.1812*Cload+1.1677
PBCD2W	OEN->PAD (fall)	2.823	6.454	10.05	23.42	0.1789*Cload+1.0708
PBCD2W	OEN->PAD (rise)	2.97	6.625	10.25	23.77	0.1807*Cload+1.1911

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCD4W	PAD->C (fall)	0.2876	0.2929	0.2958	0.3068	0.2331*Cload+0.2876

PBCD4W	PAD->C (rise)	0.3432	0.3456	0.3511	0.3596	0.1559*Cload+0.3444

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCD4W	I->PAD (fall)	1.822	3.63	5.427	12.13	0.0895*Cload+0.9416
PBCD4W	I->PAD (rise)	1.744	3.597	5.427	12.22	0.0910*Cload+0.8557
PBCD4W	OEN->PAD (fall)	1.727	3.535	5.332	12.04	0.0896*Cload+0.8425
PBCD4W	OEN->PAD (rise)	1.774	3.613	5.432	12.21	0.0907*Cload+0.8821

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCD8W	PAD->C (fall)	0.2877	0.2931	0.2959	0.3069	0.2346*Cload+0.2877
PBCD8W	PAD->C (rise)	0.3435	0.346	0.3511	0.3636	0.2145*Cload+0.3435

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCD8W	I->PAD (fall)	1.288	2.197	3.093	6.444	0.0448*Cload+0.8475
PBCD8W	I->PAD (rise)	1.227	2.16	3.079	6.491	0.0457*Cload+0.7828
PBCD8W	OEN->PAD (fall)	1.239	2.144	3.041	6.391	0.0447*Cload+0.8011
PBCD8W	OEN->PAD (rise)	1.254	2.182	3.097	6.497	0.0455*Cload+0.8118

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCD12W	PAD->C (fall)	0.2876	0.2929	0.2958	0.3068	0.2331*Cload+0.2876
PBCD12W	PAD->C (rise)	0.3435	0.346	0.3511	0.3636	0.2145*Cload+0.3435

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCD12W	I->PAD (fall)	1.131	1.74	2.338	4.571	0.0299*Cload+0.8378
PBCD12W	I->PAD (rise)	1.085	1.718	2.333	4.613	0.0306*Cload+0.7925
PBCD12W	OEN->PAD (fall)	1.097	1.701	2.299	4.53	0.0298*Cload+0.805
PBCD12W	OEN->PAD (rise)	1.106	1.735	2.348	4.621	0.0305*Cload+0.8131

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCD16W	PAD->C (fall)	0.2877	0.2931	0.2959	0.3069	0.2346*Cload+0.2877

PBCD16W	PAD->C (rise)	0.3435	0.346	0.3511	0.3636	0.2145*Cload+0.3435

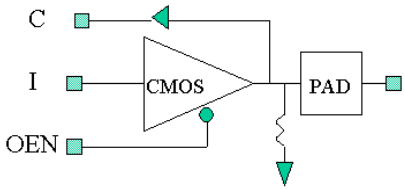
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCD16W	I->PAD (fall)	1.07	1.527	1.977	3.652	0.0224*Cload+0.8525
PBCD16W	I->PAD (rise)	1.035	1.525	1.991	3.704	0.0231*Cload+0.8221
PBCD16W	OEN->PAD (fall)	1.041	1.496	1.944	3.618	0.0224*Cload+0.8207
PBCD16W	OEN->PAD (rise)	1.053	1.54	2.003	3.712	0.0231*Cload+0.8353

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCD24W	PAD->C (fall)	0.2878	0.2904	0.2963	0.3096	0.2274*Cload+0.2880
PBCD24W	PAD->C (rise)	0.3402	0.3425	0.3467	0.3557	0.1616*Cload+0.3406

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCD24W	I->PAD (fall)	1.131	1.45	1.752	2.87	0.0151*Cload+0.9891
PBCD24W	I->PAD (rise)	1.094	1.453	1.774	2.925	0.0158*Cload+0.9622
PBCD24W	OEN->PAD (fall)	1.107	1.425	1.727	2.843	0.0150*Cload+0.9692
PBCD24W	OEN->PAD (rise)	1.1	1.456	1.775	2.923	0.0158*Cload+0.9642

PBDxW

CMOS 3-STATE OUTPUT PAD WITH INPUT and PULLDOWN, 5V-Tolerant



● Truth Table

Input			Output
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	0
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBD2W	1	161.1
PBD4W	1	165.4
PBD8W	1	173
PBD12W	1	179.5
PBD16W	1	186.7
PBD24W	1	197

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBD2W				
PBD4W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD2W	PAD->C (fall)	0.2839	0.2862	0.2917	0.3045	0.2160*Cload+0.2840
PBD2W	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD2W	I->PAD (fall)	2.962	6.56	10.13	23.38	0.1773*Cload+1.2281
PBD2W	I->PAD (rise)	2.958	6.655	10.3	23.87	0.1817*Cload+1.1793
PBD2W	OEN->PAD (fall)	2.701	6.313	9.892	23.19	0.178*Cload+0.9565
PBD2W	OEN->PAD (rise)	2.98	6.647	10.28	23.85	0.1814*Cload+1.189

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD4W	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBD4W	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD4W	I->PAD (fall)	1.814	3.615	5.404	12.08	0.0892*Cload+0.9337
PBD4W	I->PAD (rise)	1.748	3.603	5.436	12.24	0.0911*Cload+0.8601
PBD4W	OEN->PAD (fall)	1.67	3.472	5.265	11.95	0.0893*Cload+0.7893
PBD4W	OEN->PAD (rise)	1.777	3.619	5.441	12.23	0.0908*Cload+0.8862

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD8W	PAD->C (fall)	0.2841	0.2897	0.292	0.3033	0.2417*Cload+0.2838
PBD8W	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD8W	I->PAD (fall)	1.286	2.192	3.087	6.43	0.0447*Cload+0.8461
PBD8W	I->PAD (rise)	1.228	2.161	3.081	6.496	0.0457*Cload+0.7851
PBD8W	OEN->PAD (fall)	1.211	2.115	3.01	6.356	0.0447*Cload+0.7703
PBD8W	OEN->PAD (rise)	1.255	2.184	3.099	6.503	0.0456*Cload+0.8092

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD12W	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBD12W	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD12W	I->PAD (fall)	1.13	1.738	2.335	4.564	0.0298*Cload+0.84
PBD12W	I->PAD (rise)	1.085	1.718	2.334	4.616	0.0306*Cload+0.7935
PBD12W	OEN->PAD (fall)	1.078	1.682	2.279	4.509	0.0298*Cload+0.7852
PBD12W	OEN->PAD (rise)	1.106	1.736	2.35	4.624	0.0305*Cload+0.8146

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD16W	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBD16W	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

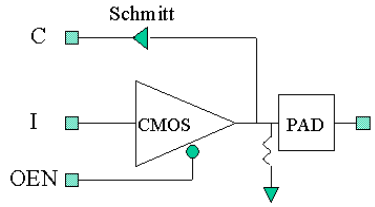
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD16W	I->PAD (fall)	1.07	1.526	1.976	3.648	0.0224*Cload+0.851
PBD16W	I->PAD (rise)	1.035	1.526	1.991	3.706	0.0232*Cload+0.8175
PBD16W	OEN->PAD (fall)	1.028	1.482	1.93	3.602	0.0223*Cload+0.8118
PBD16W	OEN->PAD (rise)	1.054	1.54	2.004	3.713	0.0231*Cload+0.8361

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBD24W	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBD24W	PAD->C (rise)	0.3471	0.3496	0.355	0.3678	0.2188*Cload+0.3472

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBD24W	I->PAD (fall)	1.13	1.449	1.752	2.868	0.0151*Cload+0.9881
PBD24W	I->PAD (rise)	1.095	1.453	1.774	2.926	0.0158*Cload+0.9627
PBD24W	OEN->PAD (fall)	1.097	1.416	1.717	2.833	0.0151*Cload+0.9541
PBD24W	OEN->PAD (rise)	1.1	1.456	1.775	2.924	0.0158*Cload+0.9645

PBSDxW

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLDOWN, 5V-Tolerant



● Truth Table

Input			Output
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	0
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBSD2W	1	161.4
PBSD4W	1	166.9
PBSD8W	1	174.1
PBSD12W	1	178.4
PBSD16W	1	189
PBSD24W	1	197

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSD2W				
PBSD4W				
PBSD8W				
PBSD12W				
PBSD16W				
PBSD24W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSD2W	PAD->C (fall)	0.4509	0.4538	0.4584	0.4681	0.1802*Cload+0.4515
PBSD2W	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD2W	I->PAD (fall)	2.962	6.56	10.13	23.38	0.1773*Cload+1.2281
PBSD2W	I->PAD (rise)	2.953	6.649	10.29	23.87	0.1818*Cload+1.1687
PBSD2W	OEN->PAD (fall)	2.701	6.312	9.891	23.19	0.178*Cload+0.9560
PBSD2W	OEN->PAD (rise)	2.975	6.642	10.28	23.85	0.1814*Cload+1.1865

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSD4W	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSD4W	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD4W	I->PAD (fall)	1.814	3.615	5.404	12.08	0.0892*Cload+0.9337
PBSD4W	I->PAD (rise)	1.746	3.601	5.433	12.24	0.0911*Cload+0.8583
PBSD4W	OEN->PAD (fall)	1.669	3.472	5.264	11.95	0.0893*Cload+0.7888
PBSD4W	OEN->PAD (rise)	1.775	3.616	5.439	12.23	0.0908*Cload+0.8844

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSD8W	PAD->C (fall)	0.4552	0.4577	0.4635	0.4766	0.2231*Cload+0.4554
PBSD8W	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD8W	I->PAD (fall)	1.286	2.192	3.087	6.43	0.0447*Cload+0.8461
PBSD8W	I->PAD (rise)	1.228	2.16	3.08	6.495	0.0457*Cload+0.7843
PBSD8W	OEN->PAD (fall)	1.211	2.115	3.01	6.356	0.0447*Cload+0.7703
PBSD8W	OEN->PAD (rise)	1.254	2.183	3.098	6.501	0.0456*Cload+0.808

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL12W	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSDL12W	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD12W	I->PAD (fall)	1.13	1.738	2.335	4.565	0.0298*Cload+0.8402
PBSD12W	I->PAD (rise)	1.085	1.718	2.334	4.615	0.0306*Cload+0.7932
PBSD12W	OEN->PAD (fall)	1.078	1.682	2.279	4.509	0.0298*Cload+0.7852
PBSD12W	OEN->PAD (rise)	1.106	1.736	2.349	4.623	0.0305*Cload+0.8141

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL16W	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSDL16W	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

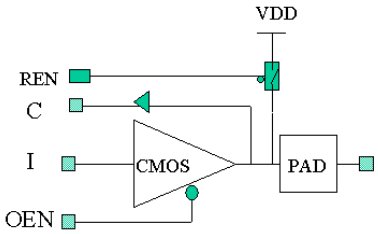
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD16W	I->PAD (fall)	1.07	1.526	1.976	3.648	0.0224*Cload+0.851
PBSD16W	I->PAD (rise)	1.035	1.525	1.991	3.705	0.0232*Cload+0.817
PBSD16W	OEN->PAD (fall)	1.027	1.481	1.93	3.602	0.0223*Cload+0.8113
PBSD16W	OEN->PAD (rise)	1.053	1.54	2.003	3.713	0.0231*Cload+0.8356

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSD24W	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSD24W	PAD->C (rise)	0.4989	0.5014	0.5056	0.5143	0.1602*Cload+0.4994

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSD24W	I->PAD (fall)	1.13	1.449	1.751	2.868	0.0151*Cload+0.9878
PBSD24W	I->PAD (rise)	1.094	1.453	1.774	2.925	0.0158*Cload+0.9622
PBSD24W	OEN->PAD (fall)	1.097	1.415	1.717	2.833	0.0150*Cload+0.9592
PBSD24W	OEN->PAD (rise)	1.099	1.456	1.775	2.923	0.0158*Cload+0.964

PBCUxW

CMOS 3-STATE OUTPUT PAD WITH INPUT and CONTROLLABLE PULLUP, 5V-Tolerant



● Truth Table

Input				Output
REN	OEN	I	PAD	C
x	1	x	0	0
x	1	x	1	1
0	1	x	pull-up	1
1	1	x	Z	x
x	0	0	0	0
x	0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBCU2W	1	86.78
PBCU4W	1	85.77
PBCU8W	1	95.08
PBCU12W	1	100.4
PBCU16W	1	112.8
PBCU24W	1	125.4

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBCU2W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU2W	PAD->C (fall)	0.2951	0.2974	0.302	0.3126	0.1845*Cload+0.2953
PBCU2W	PAD->C (rise)	0.3434	0.3458	0.3513	0.3598	0.1559*Cload+0.3446

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU2W	I->PAD (fall)	2.989	6.618	10.22	23.59	0.1789*Cload+1.2383
PBCU2W	I->PAD (rise)	2.948	6.633	10.26	23.79	0.1812*Cload+1.1682
PBCU2W	OEN->PAD (fall)	2.824	6.455	10.05	23.42	0.1789*Cload+1.0713
PBCU2W	OEN->PAD (rise)	2.97	6.626	10.25	23.77	0.1808*Cload+1.186

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU4W	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCU4W	PAD->C (rise)	0.3434	0.3458	0.3513	0.3598	0.1559*Cload+0.3446

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU4W	I->PAD (fall)	1.822	3.63	5.427	12.13	0.0895*Cload+0.9416
PBCU4W	I->PAD (rise)	1.745	3.598	5.427	12.22	0.0910*Cload+0.8562
PBCU4W	OEN->PAD (fall)	1.728	3.535	5.332	12.04	0.0896*Cload+0.8427
PBCU4W	OEN->PAD (rise)	1.775	3.613	5.433	12.21	0.0906*Cload+0.888

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU8W	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCU8W	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU8W	I->PAD (fall)	1.288	2.197	3.094	6.444	0.0448*Cload+0.8477
PBCU8W	I->PAD (rise)	1.227	2.16	3.079	6.491	0.0457*Cload+0.7828
PBCU8W	OEN->PAD (fall)	1.239	2.144	3.041	6.391	0.0447*Cload+0.8011
PBCU8W	OEN->PAD (rise)	1.254	2.182	3.097	6.498	0.0455*Cload+0.8121

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU12W	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCU12W	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU12W	I->PAD (fall)	1.131	1.74	2.338	4.571	0.0299*Cload+0.8378
PBCU12W	I->PAD (rise)	1.085	1.718	2.333	4.613	0.0306*Cload+0.7925
PBCU12W	OEN->PAD (fall)	1.097	1.701	2.299	4.531	0.0298*Cload+0.8052
PBCU12W	OEN->PAD (rise)	1.106	1.736	2.349	4.622	0.0305*Cload+0.8138

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCU16W	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCU16W	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCU16W	I->PAD (fall)	1.07	1.527	1.978	3.652	0.0224*Cload+0.8527

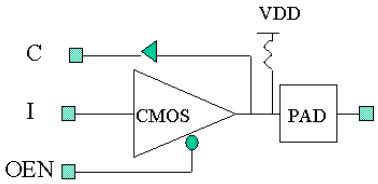
PBCU16W	I->PAD (rise)	1.035	1.525	1.991	3.705 0.0232*Cload+0.817
PBCU16W	OEN->PAD (fall)	1.041	1.496	1.945	3.618 0.0224*Cload+0.821
PBCU16W	OEN->PAD (rise)	1.053	1.54	2.003	3.712 0.0231*Cload+0.8353

cell	delay_path	Standard Load			Performance Equation
		2	4	8	16
PBCU24W	PAD->C (fall)	0.2895	0.2924	0.2988	0.312 0.2303*Cload+0.2901
PBCU24W	PAD->C (rise)	0.3401	0.3425	0.3467	0.3557 0.1630*Cload+0.3405

cell	delay_path	Sample Loads(pf)			Performance Equation
		10	30	50	125
PBCU24W	I->PAD (fall)	1.131	1.45	1.752	2.87 0.0151*Cload+0.9891
PBCU24W	I->PAD (rise)	1.094	1.453	1.774	2.925 0.0158*Cload+0.9622
PBCU24W	OEN->PAD (fall)	1.107	1.425	1.727	2.843 0.0150*Cload+0.9692
PBCU24W	OEN->PAD (rise)	1.099	1.456	1.775	2.923 0.0158*Cload+0.964

PBUxW

CMOS 3-STATE OUTPUT PAD WITH INPUT and PULLUP, 5V-Tolerant



● Truth Table

Input			Output
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	1
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PBU2W	1	186.7
PBU4W	1	191.9
PBU8W	1	201.1
PBU12W	1	206.8
PBU16W	1	212
PBU24W	1	229.5

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBU2W				
PBU4W				
PBU8W				
PBU12W				
PBU16W				
PBU24W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU2W	PAD->C (fall)	0.297	0.2992	0.3042	0.316	0.2002*Cload+0.2971
PBU2W	PAD->C (rise)	0.339	0.3408	0.3511	0.359	0.1387*Cload+0.3426

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU2W	I->PAD (fall)	3.011	6.672	10.3	23.76	0.1802*Cload+1.25
PBU2W	I->PAD (rise)	2.923	6.571	10.17	23.56	0.1793*Cload+1.1686
PBU2W	OEN->PAD (fall)	2.847	6.508	10.13	23.59	0.1802*Cload+1.083
PBU2W	OEN->PAD (rise)	2.883	6.516	10.11	23.55	0.1797*Cload+1.1058

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU4W	PAD->C (fall)	0.2943	0.2965	0.3014	0.3129	0.1959*Cload+0.2944
PBU4W	PAD->C (rise)	0.339	0.3408	0.3511	0.359	0.1387*Cload+0.3426

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU4W	I->PAD (fall)	1.827	3.644	5.449	12.18	0.0899*Cload+0.9428
PBU4W	I->PAD (rise)	1.738	3.582	5.403	12.16	0.0905*Cload+0.8563
PBU4W	OEN->PAD (fall)	1.733	3.549	5.353	12.08	0.0899*Cload+0.8466
PBU4W	OEN->PAD (rise)	1.734	3.568	5.381	12.14	0.0904*Cload+0.8467

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU8W	PAD->C (fall)	0.2918	0.2945	0.3006	0.3139	0.2288*Cload+0.2922
PBU8W	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU8W	I->PAD (fall)	1.289	2.2	3.099	6.456	0.0449*Cload+0.8476
PBU8W	I->PAD (rise)	1.225	2.156	3.073	6.476	0.0456*Cload+0.7815
PBU8W	OEN->PAD (fall)	1.24	2.148	3.046	6.403	0.0448*Cload+0.8012
PBU8W	OEN->PAD (rise)	1.234	2.161	3.075	6.471	0.0455*Cload+0.7896

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU12W	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBU12W	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU12W	I->PAD (fall)	1.131	1.741	2.341	4.576	0.0299*Cload+0.8401
PBU12W	I->PAD (rise)	1.084	1.716	2.33	4.607	0.0306*Cload+0.7895
PBU12W	OEN->PAD (fall)	1.097	1.702	2.301	4.536	0.0298*Cload+0.8072
PBU12W	OEN->PAD (rise)	1.091	1.722	2.334	4.606	0.0305*Cload+0.7988

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU16W	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBU16W	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

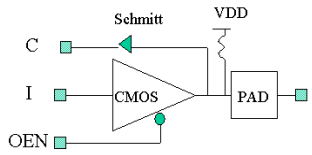
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU16W	I->PAD (fall)	1.071	1.528	1.979	3.655	0.0224*Cload+0.8542
PBU16W	I->PAD (rise)	1.034	1.524	1.989	3.701	0.0231*Cload+0.8203
PBU16W	OEN->PAD (fall)	1.042	1.497	1.946	3.621	0.0224*Cload+0.8225
PBU16W	OEN->PAD (rise)	1.042	1.53	1.993	3.701	0.0231*Cload+0.8248

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBU24W	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBU24W	PAD->C (rise)	0.3393	0.3417	0.3459	0.3547	0.1602*Cload+0.3398

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBU24W	I->PAD (fall)	1.131	1.45	1.753	2.872	0.0151*Cload+0.9898
PBU24W	I->PAD (rise)	1.094	1.452	1.773	2.923	0.0158*Cload+0.9612
PBU24W	OEN->PAD (fall)	1.107	1.425	1.727	2.845	0.0151*Cload+0.9643
PBU24W	OEN->PAD (rise)	1.09	1.449	1.768	2.916	0.0158*Cload+0.9565

PBSUxW

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLUP, 5V-Tolerant



● Truth Table

Input			Output
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	1
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBSU2W	1	189.6
PBSU4W	1	210.4
PBSU8W	1	198.2
PBSU12W	1	206.6
PBSU16W	1	212.7
PBSU24W	1	227.9

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSU2W				
PBSU4W				
PBSU8W				
PBSU12W				
PBSU16W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU2W	PAD->C (fall)	0.4561	0.459	0.4653	0.4785	0.2303*Cload+0.4566
PBSU2W	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU2W	I->PAD (fall)	3.009	6.669	10.29	23.76	0.1803*Cload+1.2408
PBSU2W	I->PAD (rise)	2.918	6.565	10.16	23.56	0.1794*Cload+1.158
PBSU2W	OEN->PAD (fall)	2.844	6.505	10.13	23.59	0.1802*Cload+1.0815
PBSU2W	OEN->PAD (rise)	2.878	6.511	10.11	23.54	0.1796*Cload+1.1062

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU4W	PAD->C (fall)	0.456	0.4583	0.4631	0.4742	0.1917*Cload+0.4562
PBSU4W	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU4W	I->PAD (fall)	1.826	3.642	5.447	12.18	0.0899*Cload+0.9416
PBSU4W	I->PAD (rise)	1.736	3.58	5.4	12.16	0.0905*Cload+0.8546
PBSU4W	OEN->PAD (fall)	1.732	3.547	5.352	12.08	0.0899*Cload+0.8456
PBSU4W	OEN->PAD (rise)	1.731	3.565	5.379	12.14	0.0904*Cload+0.8447

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU8W	PAD->C (fall)	0.4608	0.4631	0.4684	0.4811	0.2145*Cload+0.4608
PBSU8W	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU8W	I->PAD (fall)	1.288	2.199	3.098	6.456	0.0449*Cload+0.8468
PBSU8W	I->PAD (rise)	1.225	2.155	3.072	6.475	0.0456*Cload+0.7807
PBSU8W	OEN->PAD (fall)	1.24	2.147	3.046	6.403	0.0448*Cload+0.801
PBSU8W	OEN->PAD (rise)	1.233	2.16	3.073	6.469	0.0455*Cload+0.7881

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU12W	PAD->C (fall)	0.4615	0.4637	0.4686	0.48	0.1945*Cload+0.4616
PBSU12W	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU12W	I->PAD (fall)	1.131	1.741	2.34	4.576	0.0299*Cload+0.8398
PBSU12W	I->PAD (rise)	1.083	1.715	2.33	4.606	0.0306*Cload+0.7887
PBSU12W	OEN->PAD (fall)	1.097	1.702	2.301	4.536	0.0298*Cload+0.8072
PBSU12W	OEN->PAD (rise)	1.09	1.721	2.334	4.605	0.0305*Cload+0.7981

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU16W	PAD->C (fall)	0.4615	0.4637	0.4686	0.48	0.1945*Cload+0.4616
PBSU16W	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

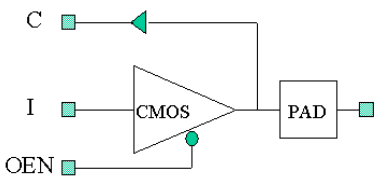
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU16W	I->PAD (fall)	1.071	1.528	1.978	3.655	0.0224*Cload+0.854
PBSU16W	I->PAD (rise)	1.034	1.523	1.988	3.7	0.0231*Cload+0.8196
PBSU16W	OEN->PAD (fall)	1.042	1.496	1.946	3.621	0.0224*Cload+0.8222
PBSU16W	OEN->PAD (rise)	1.041	1.529	1.992	3.701	0.0231*Cload+0.8241

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSU24W	PAD->C (fall)	0.4615	0.4637	0.4686	0.48	0.1945*Cload+0.4616
PBSU24W	PAD->C (rise)	0.4927	0.4949	0.4996	0.5111	0.1959*Cload+0.4927

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSU24W	I->PAD (fall)	1.131	1.45	1.753	2.871	0.0151*Cload+0.9896
PBSU24W	I->PAD (rise)	1.093	1.452	1.772	2.923	0.0158*Cload+0.9607
PBSU24W	OEN->PAD (fall)	1.107	1.425	1.727	2.844	0.0151*Cload+0.9641
PBSU24W	OEN->PAD (rise)	1.089	1.448	1.767	2.916	0.0158*Cload+0.9557

PBLxW

CMOS 3-STATE OUTPUT WITH PAD INPUT and LIMITED SLEW RATE , , 5V-Tolerant



● Truth Table

Input		Output	
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBL8W	1	96.32
PBL12W	1	100
PBL16W	1	110.7
PBL24W	1	125.9

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBL8W				

PBLxW

CMOS 3-STATE OUTPUT WITH PAD INPUT and LIMITED SLEW RATE , , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBL8W	PAD->C (fall)	0.288	0.2936	0.2961	0.3073	0.2403*Cload+0.2878
PBL8W	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBL8W	I->PAD (fall)	1.467	2.377	3.274	6.625	0.0448*Cload+1.0277
PBL8W	I->PAD (rise)	1.421	2.355	3.275	6.687	0.0457*Cload+0.9781
PBL8W	OEN->PAD (fall)	1.419	2.327	3.223	6.573	0.0448*Cload+0.9775
PBL8W	OEN->PAD (rise)	1.435	2.366	3.281	6.682	0.0456*Cload+0.99

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBL12W	PAD->C (fall)	0.2878	0.2933	0.296	0.3071	0.2374*Cload+0.2877
PBL12W	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBL12W	I->PAD (fall)	1.216	1.826	2.425	4.657	0.0299*Cload+0.9238
PBL12W	I->PAD (rise)	1.168	1.802	2.417	4.698	0.0306*Cload+0.8765

PBL12W	OEN->PAD (fall)	1.18	1.787	2.385	4.617	0.0298*Cload+0.8905
PBL12W	OEN->PAD (rise)	1.183	1.814	2.428	4.701	0.0305*Cload+0.8921

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBL16W	PAD->C (fall)	0.288	0.2936	0.2961	0.3073	0.2403*Cload+0.2878
PBL16W	PAD->C (rise)	0.3432	0.3458	0.3505	0.3632	0.2188*Cload+0.3430

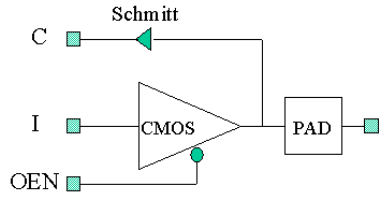
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBL16W	I->PAD (fall)	1.616	2.133	2.599	4.282	0.0231*Cload+1.4158
PBL16W	I->PAD (rise)	1.552	2.076	2.55	4.269	0.0236*Cload+1.3432
PBL16W	OEN->PAD (fall)	1.574	2.093	2.56	4.243	0.0231*Cload+1.3758
PBL16W	OEN->PAD (rise)	1.539	2.063	2.537	4.252	0.0235*Cload+1.3346

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBL24W	PAD->C (fall)	0.288	0.2906	0.2966	0.3099	0.2274*Cload+0.2883
PBL24W	PAD->C (rise)	0.3399	0.3422	0.3464	0.3554	0.1616*Cload+0.3403

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBL24W	I->PAD (fall)	1.575	1.974	2.306	3.453	0.0162*Cload+1.4562
PBL24W	I->PAD (rise)	1.536	1.938	2.277	3.444	0.0165*Cload+1.4118
PBL24W	OEN->PAD (fall)	1.547	1.95	2.283	3.431	0.0163*Cload+1.4266
PBL24W	OEN->PAD (rise)	1.51	1.914	2.253	3.419	0.0165*Cload+1.3871

PBSLxW

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and LIMITED SLEW RATE , , 5V-Toleran



● Truth Table

Input			Output
OEN	I	PAD	C
1	x	0	0
1	x	1	1
1	x	Z	x
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PBSL8W	1	99.6
PBSL12W	1	101.5
PBSL16W	1	115.1
PBSL24W	1	125

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSL8W				
PBSL12W				
PBSL16W				
PBSL24W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSL8W	PAD->C (fall)	0.4508	0.4531	0.4578	0.4685	0.1859*Cload+0.4510
PBSL8W	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSL8W	I->PAD (fall)	1.467	2.377	3.273	6.624	0.0448*Cload+1.0272
PBSL8W	I->PAD (rise)	1.42	2.354	3.274	6.686	0.0457*Cload+0.9771
PBSL8W	OEN->PAD (fall)	1.418	2.326	3.222	6.573	0.0448*Cload+0.9767
PBSL8W	OEN->PAD (rise)	1.434	2.364	3.28	6.681	0.0455*Cload+0.9941

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSL12W	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636	0.1487*Cload+0.4480
PBSL12W	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSL12W	I->PAD (fall)	1.216	1.826	2.425	4.657	0.0299*Cload+0.9238
PBSL12W	I->PAD (rise)	1.167	1.801	2.417	4.697	0.0306*Cload+0.8757
PBSL12W	OEN->PAD (fall)	1.18	1.787	2.385	4.616	0.0298*Cload+0.8902
PBSL12W	OEN->PAD (rise)	1.183	1.813	2.427	4.7	0.0305*Cload+0.8913

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSL16W	PAD->C (fall)	0.4441	0.4481	0.4572	0.4636	0.1487*Cload+0.4480
PBSL16W	PAD->C (rise)	0.495	0.498	0.5026	0.5108	0.1602*Cload+0.4960

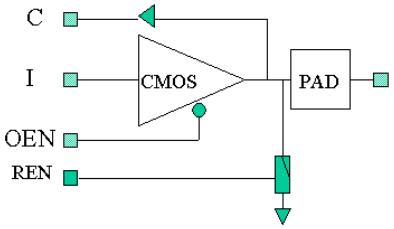
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSL16W	I->PAD (fall)	1.616	2.132	2.598	4.282	0.0231*Cload+1.4153
PBSL16W	I->PAD (rise)	1.551	2.075	2.549	4.268	0.0236*Cload+1.3422
PBSL16W	OEN->PAD (fall)	1.574	2.093	2.559	4.243	0.0231*Cload+1.3756
PBSL16W	OEN->PAD (rise)	1.538	2.063	2.536	4.252	0.0235*Cload+1.3341

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSL24W	PAD->C (fall)	0.4466	0.449	0.4548	0.4678	0.2203*Cload+0.4468
PBSL24W	PAD->C (rise)	0.4931	0.4953	0.5001	0.5119	0.2002*Cload+0.4931

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSL24W	I->PAD (fall)	1.575	1.973	2.306	3.453	0.0162*Cload+1.456
PBSL24W	I->PAD (rise)	1.535	1.938	2.277	3.443	0.0165*Cload+1.4113
PBSL24W	OEN->PAD (fall)	1.547	1.95	2.283	3.43	0.0163*Cload+1.4263
PBSL24W	OEN->PAD (rise)	1.51	1.914	2.253	3.419	0.0165*Cload+1.3871

PBCDLxW

CMOS 3-STATE OUTPUT PAD WITH INPUT CONTROLLABLE PULLDOWN, and LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

Input				Output
REN	**OEN**	**I**	**PAD**	**C**
x	1	x	0	0
x	1	x	1	1
0	1	x	pull-down	0
1	1	x	Z	x
x	0	0	0	0
x	0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PBCDL8W	**1**	**93.45**
PBCDL12W	**1**	**100.5**
PBCDL16W	**1**	**109.2**
PBCDL24W	**1**	**137.7**

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBCDL8W				
PBCDL12W				
PBCDL16W				
PBCDL24W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCDL8W	PAD->C (fall)	0.2877	0.2931	0.2959	0.3069	0.2346*Cload+0.2877
PBCDL8W	PAD->C (rise)	0.3435	0.346	0.3511	0.3636	0.2145*Cload+0.3435

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCDL8W	I->PAD (fall)	1.467	2.377	3.274	6.624	0.0448*Cload+1.0275
PBCDL8W	I->PAD (rise)	1.421	2.355	3.275	6.687	0.0457*Cload+0.9781
PBCDL8W	OEN->PAD (fall)	1.419	2.327	3.223	6.573	0.0448*Cload+0.9775
PBCDL8W	OEN->PAD (rise)	1.435	2.366	3.281	6.682	0.0456*Cload+0.99

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCDL12W	PAD->C (fall)	0.2876	0.2929	0.2958	0.3068	0.2331*Cload+0.2876
PBCDL12W	PAD->C (rise)	0.3435	0.346	0.3511	0.3636	0.2145*Cload+0.3435

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCDL12W	I->PAD (fall)	1.216	1.826	2.425	4.657	0.0299*Cload+0.9238
PBCDL12W	I->PAD (rise)	1.168	1.802	2.417	4.698	0.0306*Cload+0.8765
PBCDL12W	OEN->PAD (fall)	1.18	1.787	2.385	4.617	0.0298*Cload+0.8905
PBCDL12W	OEN->PAD (rise)	1.183	1.814	2.428	4.701	0.0305*Cload+0.8921

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCDL16W	PAD->C (fall)	0.2877	0.2931	0.2959	0.3069	0.2346*Cload+0.2877
PBCDL16W	PAD->C (rise)	0.3435	0.346	0.3511	0.3636	0.2145*Cload+0.3435

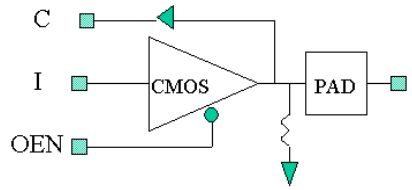
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCDL16W	I->PAD (fall)	1.616	2.133	2.599	4.282	0.0231*Cload+1.4158
PBCDL16W	I->PAD (rise)	1.552	2.076	2.55	4.269	0.0236*Cload+1.3432
PBCDL16W	OEN->PAD (fall)	1.574	2.093	2.56	4.243	0.0231*Cload+1.3758
PBCDL16W	OEN->PAD (rise)	1.539	2.063	2.537	4.252	0.0235*Cload+1.3346

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCDL24W	PAD->C (fall)	0.2878	0.2904	0.2963	0.3096	0.2274*Cload+0.2880
PBCDL24W	PAD->C (rise)	0.3402	0.3425	0.3467	0.3557	0.1616*Cload+0.3406

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCDL24W	I->PAD (fall)	1.575	1.974	2.306	3.453	0.0162*Cload+1.4562
PBCDL24W	I->PAD (rise)	1.536	1.938	2.277	3.444	0.0165*Cload+1.4118
PBCDL24W	OEN->PAD (fall)	1.547	1.95	2.283	3.431	0.0163*Cload+1.4266
PBCDL24W	OEN->PAD (rise)	1.51	1.914	2.253	3.419	0.0165*Cload+1.3871

PBDLxW

CMOS 3-STATE OUTPUT PAD WITH INPUT PULLDOWN and LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

Input		Output	
OEN	**I**	**PAD**	**C**
1	x	0	0
1	x	1	1
1	x	Z	0
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBDL8W	**1**	**169.1**
PBDL12W	**1**	**175.4**
PBDL16W	**1**	**183.1**
PBDL24W	**1**	**192**

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBDL8W				
PBDL12W				
PBDL16W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBDL8W	PAD->C (fall)	0.2841	0.2897	0.292	0.3033	0.2417*Cload+0.2838
PBDL8W	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBDL8W	I->PAD (fall)	1.465	2.373	3.267	6.611	0.0447*Cload+1.0263
PBDL8W	I->PAD (rise)	1.422	2.357	3.277	6.692	0.0457*Cload+0.9806
PBDL8W	OEN->PAD (fall)	1.39	2.297	3.192	6.538	0.0447*Cload+0.9516
PBDL8W	OEN->PAD (rise)	1.436	2.367	3.283	6.687	0.0456*Cload+0.9922

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBDL12W	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBDL12W	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBDL12W	I->PAD (fall)	1.215	1.824	2.422	4.651	0.0298*Cload+0.9262
PBDL12W	I->PAD (rise)	1.168	1.803	2.419	4.7	0.0306*Cload+0.8777
PBDL12W	OEN->PAD (fall)	1.161	1.768	2.365	4.595	0.0298*Cload+0.8705
PBDL12W	OEN->PAD (rise)	1.184	1.815	2.429	4.703	0.0305*Cload+0.8933

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBDL16W	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBDL16W	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

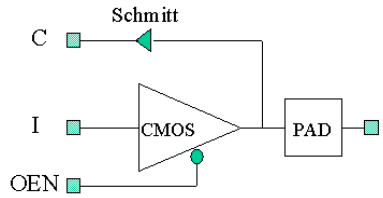
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBDL16W	I->PAD (fall)	1.616	2.131	2.596	4.278	0.0231*Cload+1.4136
PBDL16W	I->PAD (rise)	1.553	2.077	2.551	4.27	0.0236*Cload+1.3442
PBDL16W	OEN->PAD (fall)	1.556	2.078	2.545	4.227	0.0232*Cload+1.3545
PBDL16W	OEN->PAD (rise)	1.54	2.064	2.538	4.254	0.0235*Cload+1.3358

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBDL24W	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PBDL24W	PAD->C (rise)	0.3471	0.3496	0.355	0.3678	0.2188*Cload+0.3472

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBDL24W	I->PAD (fall)	1.575	1.973	2.305	3.451	0.0162*Cload+1.4552
PBDL24W	I->PAD (rise)	1.536	1.939	2.278	3.444	0.0165*Cload+1.4123
PBDL24W	OEN->PAD (fall)	1.531	1.939	2.273	3.42	0.0163*Cload+1.4146
PBDL24W	OEN->PAD (rise)	1.511	1.915	2.254	3.42	0.0165*Cload+1.3881

PBSDLW

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLDOWN, and LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

Input		Output	
OEN	**I**	**PAD**	**C**
1	x	0	0
1	x	1	1
1	x	Z	0
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBSDL8W	**1**	**170.3**
PBSDL12W	**1**	**179.2**
PBSDL16W	**1**	**181.2**
PBSDL24W	**1**	**193.7**

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSDL8W				
PBSDL12W				
PBSDL16W				

PBSDLxW

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLDOWN, and LIMITED SLEW RATE , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL8W	PAD->C (fall)	0.4552	0.4577	0.4635	0.4766	0.2231*Cload+0.4554
PBSDL8W	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSDL8W	I->PAD (fall)	1.465	2.373	3.267	6.61	0.0447*Cload+1.0261
PBSDL8W	I->PAD (rise)	1.421	2.356	3.276	6.691	0.0457*Cload+0.9796
PBSDL8W	OEN->PAD (fall)	1.39	2.297	3.192	6.538	0.0447*Cload+0.9516
PBSDL8W	OEN->PAD (rise)	1.435	2.366	3.282	6.686	0.0456*Cload+0.9912

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL12W	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSDL12W	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSDL12W	I->PAD (fall)	1.214	1.824	2.422	4.651	0.0298*Cload+0.926
PBSDL12W	I->PAD (rise)	1.168	1.802	2.418	4.699	0.0306*Cload+0.877
PBSDL12W	OEN->PAD (fall)	1.161	1.768	2.365	4.595	0.0298*Cload+0.8705

PBSDL12W	OEN->PAD (rise)	1.183	1.814	2.428	4.702	0.0305*Cload+0.8923

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL16W	PAD->C (fall)	0.4516	0.4543	0.4588	0.4687	0.1802*Cload+0.4520
PBSDL16W	PAD->C (rise)	0.4996	0.502	0.5062	0.515	0.1602*Cload+0.5001

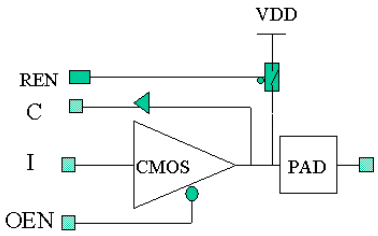
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSDL16W	I->PAD (fall)	1.615	2.131	2.596	4.278	0.0231*Cload+1.4133
PBSDL16W	I->PAD (rise)	1.552	2.076	2.55	4.27	0.0236*Cload+1.3435
PBSDL16W	OEN->PAD (fall)	1.556	2.078	2.544	4.227	0.0232*Cload+1.3542
PBSDL16W	OEN->PAD (rise)	1.539	2.064	2.537	4.253	0.0235*Cload+1.3351

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSDL24W	PAD->C (fall)	0.4523	0.4549	0.4594	0.4694	0.1802*Cload+0.4527
PBSDL24W	PAD->C (rise)	0.4989	0.5014	0.5056	0.5143	0.1602*Cload+0.4994

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSDL24W	I->PAD (fall)	1.574	1.973	2.305	3.451	0.0162*Cload+1.455
PBSDL24W	I->PAD (rise)	1.536	1.938	2.277	3.444	0.0165*Cload+1.4118
PBSDL24W	OEN->PAD (fall)	1.531	1.939	2.272	3.42	0.0163*Cload+1.4143
PBSDL24W	OEN->PAD (rise)	1.51	1.914	2.253	3.419	0.0165*Cload+1.3871

PBCULxW

CMOS 3-STATE OUTPUT PAD WITH INPUT and CONTROLLABLE PULLUP,and LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

Input				Output
REN	**OEN**	**I**	**PAD**	**C**
x	1	x	0	0
x	1	x	1	1
0	1	x	pull-up	1
1	1	x	Z	x
x	0	0	0	0
x	0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PBCUL8W	**1**	**95.77**
PBCUL12W	**1**	**96.31**
PBCUL16W	**1**	**97.03**
PBCUL24W	**1**	**130.3**

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD

PBCULxW

CMOS 3-STATE OUTPUT PAD WITH INPUT and CONTROLLABLE PULLUP,and LIMITED SLEW RATE , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCUL8W	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCUL8W	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCUL8W	I->PAD (fall)	1.467	2.377	3.274	6.625	0.0448*Cload+1.0277
PBCUL8W	I->PAD (rise)	1.421	2.355	3.275	6.688	0.0457*Cload+0.9783
PBCUL8W	OEN->PAD (fall)	1.419	2.327	3.223	6.574	0.0448*Cload+0.9777
PBCUL8W	OEN->PAD (rise)	1.435	2.366	3.281	6.682	0.0456*Cload+0.99

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCUL12W	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCUL12W	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCUL12W	I->PAD (fall)	1.216	1.826	2.425	4.657	0.0299*Cload+0.9238

PBCUL12W	I->PAD (rise)	1.168	1.802	2.418	4.698	0.0306*Cload+0.8767
PBCUL12W	OEN->PAD (fall)	1.18	1.787	2.385	4.617	0.0298*Cload+0.8905
PBCUL12W	OEN->PAD (rise)	1.183	1.814	2.428	4.701	0.0305*Cload+0.8921

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCUL16W	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PBCUL16W	PAD->C (rise)	0.3436	0.3461	0.3511	0.3636	0.2145*Cload+0.3436

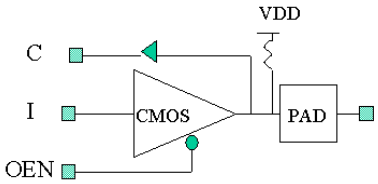
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCUL16W	I->PAD (fall)	1.616	2.133	2.599	4.283	0.0231*Cload+1.4161
PBCUL16W	I->PAD (rise)	1.552	2.076	2.55	4.269	0.0236*Cload+1.3432
PBCUL16W	OEN->PAD (fall)	1.574	2.093	2.56	4.243	0.0231*Cload+1.3758
PBCUL16W	OEN->PAD (rise)	1.539	2.063	2.537	4.252	0.0235*Cload+1.3346

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBCUL24W	PAD->C (fall)	0.2895	0.2924	0.2988	0.312	0.2303*Cload+0.2901
PBCUL24W	PAD->C (rise)	0.3401	0.3425	0.3467	0.3557	0.1630*Cload+0.3405

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBCUL24W	I->PAD (fall)	1.575	1.974	2.306	3.453	0.0162*Cload+1.4562
PBCUL24W	I->PAD (rise)	1.536	1.938	2.277	3.444	0.0165*Cload+1.4118
PBCUL24W	OEN->PAD (fall)	1.547	1.95	2.283	3.431	0.0163*Cload+1.4266
PBCUL24W	OEN->PAD (rise)	1.51	1.914	2.253	3.419	0.0165*Cload+1.3871

PBULxW

CMOS 3-STATE OUTPUT PAD WITH INPUT and PULLUP, and SLEW RATE , 5V-Tolerant



● Truth Table

Input			Output
OEN	**I**	**PAD**	**C**
1	x	0	0
1	x	1	1
1	x	Z	1
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PBUL8W	**1**	**195.8**
PBUL12W	**1**	**200.5**
PBUL16W	**1**	**216**
PBUL24W	**1**	**229.5**

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBUL8W				
PBUL12W				
PBUL16W				

PBULxW

CMOS 3-STATE OUTPUT PAD WITH INPUT and PULLUP, and SLEW RATE , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBUL8W	PAD->C (fall)	0.2918	0.2945	0.3006	0.3139	0.2288*Cload+0.2922
PBUL8W	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBUL8W	I->PAD (fall)	1.468	2.381	3.28	6.637	0.0449*Cload+1.0281
PBUL8W	I->PAD (rise)	1.419	2.351	3.268	6.672	0.0456*Cload+0.9765
PBUL8W	OEN->PAD (fall)	1.42	2.33	3.229	6.586	0.0449*Cload+0.9778
PBUL8W	OEN->PAD (rise)	1.414	2.344	3.259	6.655	0.0455*Cload+0.9723

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBUL12W	PAD->C (fall)	0.2943	0.2965	0.3014	0.3129	0.1959*Cload+0.2944
PBUL12W	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBUL12W	I->PAD (fall)	1.216	1.828	2.427	4.663	0.0299*Cload+0.9263
PBUL12W	I->PAD (rise)	1.167	1.8	2.415	4.691	0.0306*Cload+0.8735
PBUL12W	OEN->PAD (fall)	1.181	1.789	2.387	4.623	0.0299*Cload+0.8878
PBUL12W	OEN->PAD (rise)	1.169	1.8	2.414	4.685	0.0305*Cload+0.8776

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBUL16W	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBUL16W	PAD->C (rise)	0.3427	0.3453	0.3497	0.3627	0.2231*Cload+0.3423

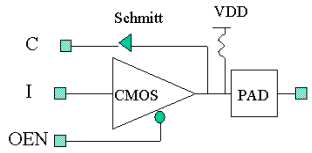
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBUL16W	I->PAD (fall)	1.617	2.134	2.6	4.286	0.0231*Cload+1.4176
PBUL16W	I->PAD (rise)	1.551	2.074	2.548	4.265	0.0235*Cload+1.3463
PBUL16W	OEN->PAD (fall)	1.575	2.095	2.561	4.247	0.0232*Cload+1.3725
PBUL16W	OEN->PAD (rise)	1.525	2.052	2.526	4.241	0.0236*Cload+1.3175

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBUL24W	PAD->C (fall)	0.29	0.2924	0.298	0.311	0.2203*Cload+0.2901
PBUL24W	PAD->C (rise)	0.3393	0.3417	0.3459	0.3547	0.1602*Cload+0.3398

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBUL24W	I->PAD (fall)	1.576	1.974	2.307	3.455	0.0162*Cload+1.4572
PBUL24W	I->PAD (rise)	1.535	1.937	2.276	3.442	0.0165*Cload+1.4106
PBUL24W	OEN->PAD (fall)	1.548	1.951	2.284	3.432	0.0163*Cload+1.4276
PBUL24W	OEN->PAD (rise)	1.498	1.906	2.245	3.412	0.0165*Cload+1.3783

PBSULxW

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLUP, and SLEW RATE , 5V-Tolerant



● Truth Table

Input			Output
OEN	**I**	**PAD**	**C**
1	x	0	0
1	x	1	1
1	x	Z	1
0	0	0	0
0	1	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PBSUL8W	**1**	**202.9**
PBSUL12W	**1**	**207.2**
PBSUL16W	**1**	**211.3**
PBSUL24W	**1**	**230.9**

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
PBSUL8W				

PBSULxW

CMOS 3-STATE OUTPUT PAD WITH SCHMITT TRIGGER INPUT and PULLUP, and SLEW RATE , 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSUL8W	PAD->C (fall)	0.4608	0.4631	0.4684	0.4811	0.2145*Cload+0.4608
PBSUL8W	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSUL8W	I->PAD (fall)	1.468	2.38	3.279	6.636	0.0449*Cload+1.0273
PBSUL8W	I->PAD (rise)	1.418	2.35	3.267	6.671	0.0456*Cload+0.9755
PBSUL8W	OEN->PAD (fall)	1.419	2.329	3.228	6.585	0.0449*Cload+0.9768
PBSUL8W	OEN->PAD (rise)	1.413	2.343	3.257	6.654	0.0455*Cload+0.9711

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSUL12W	PAD->C (fall)	0.456	0.4583	0.4631	0.4742	0.1917*Cload+0.4562
PBSUL12W	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSUL12W	I->PAD (fall)	1.216	1.827	2.427	4.663	0.0299*Cload+0.9261
PBSUL12W	I->PAD (rise)	1.166	1.799	2.414	4.69	0.0306*Cload+0.8725

PBSUL12W	OEN->PAD (fall)	1.18	1.788	2.387	4.622	0.0299*Cload+0.8871
PBSUL12W	OEN->PAD (rise)	1.168	1.8	2.413	4.684	0.0305*Cload+0.8768

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSUL16W	PAD->C (fall)	0.4615	0.4637	0.4686	0.48	0.1945*Cload+0.4616
PBSUL16W	PAD->C (rise)	0.4944	0.4975	0.5022	0.5104	0.1616*Cload+0.4954

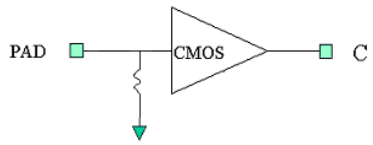
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSUL16W	I->PAD (fall)	1.617	2.134	2.6	4.285	0.0231*Cload+1.4173
PBSUL16W	I->PAD (rise)	1.55	2.074	2.547	4.264	0.0235*Cload+1.3456
PBSUL16W	OEN->PAD (fall)	1.575	2.094	2.561	4.246	0.0232*Cload+1.372
PBSUL16W	OEN->PAD (rise)	1.524	2.052	2.525	4.24	0.0236*Cload+1.3167

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PBSUL24W	PAD->C (fall)	0.4615	0.4637	0.4686	0.48	0.1945*Cload+0.4616
PBSUL24W	PAD->C (rise)	0.4927	0.4949	0.4996	0.511	0.1945*Cload+0.4927

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PBSUL24W	I->PAD (fall)	1.576	1.974	2.306	3.455	0.0162*Cload+1.457
PBSUL24W	I->PAD (rise)	1.534	1.937	2.275	3.441	0.0165*Cload+1.4098
PBSUL24W	OEN->PAD (fall)	1.548	1.951	2.284	3.432	0.0163*Cload+1.4276
PBSUL24W	OEN->PAD (rise)	1.498	1.905	2.245	3.411	0.0165*Cload+1.3778

PIDW

Input Pad With Pulldown, 5V-Tolerant



● Truth Table

Input	Output
PAD	C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PIDW	1	46.15

● Pin Capacitance (pF)

Cell Name	C	PAD
PIDW		

PIDW

Input Pad With Pulldown, 5V-Tolerant

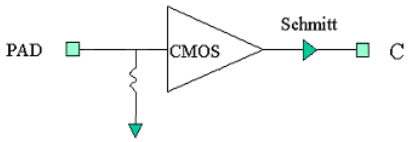
● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PIDW	PAD->C (fall)	0.2886	0.2908	0.2958	0.3076	0.2002*Cload+0.2887
PIDW	PAD->C (rise)	0.3498	0.3521	0.3577	0.3662	0.1545*Cload+0.3510

PISDW

Schmitt Trigger Input Pad, 5V-Tolerant



● Truth Table

Input PAD	Output C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PISDW	1	47.31

● Pin Capacitance (pF)

Cell Name	C	PAD
PISDW		

PISDW

Schmitt Trigger Input Pad, 5V-Tolerant

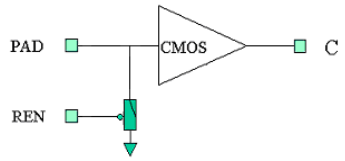
● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PISDW	PAD->C (fall)	0.3925	0.3949	0.4005	0.4134	0.2188*Cload+0.3926
PISDW	PAD->C (rise)	0.4557	0.4569	0.4649	0.4759	0.1745*Cload+0.4572

PICDW

Input Pad with Controllable Pull-down , 5V-Tolerant



● Truth Table

Input		Output
REN	**PAD**	**C**
x	1	1
x	0	0
0	pull-down	0
1	Z	x

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PICDW	**1**	**887.2**

● Pin Capacitance (pF)

Cell Name	C	PAD
PICDW		

PICDW

Input Pad with Controllable Pull-down , 5V-Tolerant

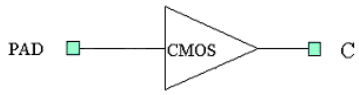
● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25℃, typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PICDW	PAD->C (fall)	0.2876	0.2929	0.2958	0.3068	0.2331*Cload+0.2876
PICDW	PAD->C (rise)	0.3432	0.3456	0.3511	0.3596	0.1559*Cload+0.3444

PIW

Input Pad , 5V-Tolerant



● Truth Table

Input	Output
PAD	C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PIW	1	50.54

● Pin Capacitance (pF)

Cell Name	C	PAD
PIW		

PIW

Input Pad, 5V-Tolerant

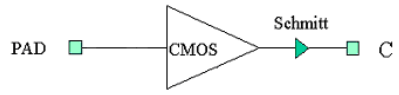
● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PIW	PAD->C (fall)	0.2878	0.2933	0.296	0.3071	0.2374*Cload+0.2877
PIW	PAD->C (rise)	0.3392	0.3452	0.3515	0.3593	0.1974*Cload+0.3419

PISW

Schmitt Trigger Input Pad, 5V-Tolerant



● Truth Table

Input	Output
PAD	C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PISW	1	46.3

● Pin Capacitance (pF)

Cell Name	C	PAD
PISW		

PISW

Schmitt Trigger Input Pad, 5V-Tolerant

● Propagation Delay(ns)

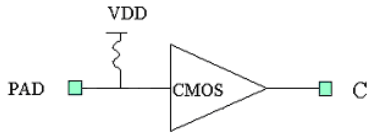
VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PISW	PAD->C (fall)	0.3826	0.3848	0.3901	0.4027	0.2117*Cload+0.3826
PISW	PAD->C (rise)	0.4529	0.4564	0.4613	0.4694	0.1659*Cload+0.4542

PIUW

PIUW

Input Pad with Pull-up , 5V-Tolerant



● Truth Table

Input	Output
PAD	**C**
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PIUW	**1**	**150.2**

● Pin Capacitance (pF)

Cell Name	C	PAD
PIUW		

PIUW

Input Pad with Pull-up , 5V-Tolerant

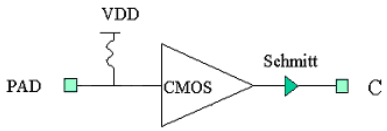
● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25℃, typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PIUW	PAD->C (fall)	0.2925	0.2948	0.2995	0.3104	0.1888*Cload+0.2927
PIUW	PAD->C (rise)	0.339	0.3408	0.3511	0.359	0.1387*Cload+0.3426

PISUW

Schmitt trigger Input Pad with Pull-up , 5V-Tolerant



● Truth Table

Input PAD	Output C
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PISUW	1	137.9

● Pin Capacitance (pF)

Cell Name	C	PAD
PISUW		

PISUW

Schmitt trigger Input Pad with Pull-up , 5V-Tolerant

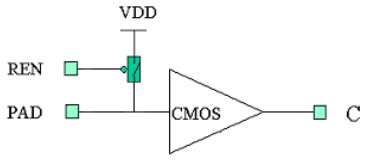
● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PISUW	PAD->C (fall)	0.4017	0.404	0.4096	0.4225	0.2174*Cload+0.4018
PISUW	PAD->C (rise)	0.4507	0.4529	0.4572	0.4664	0.1630*Cload+0.4511

PICUW

Input Pad with Controllable Pull-up , 5V-Tolerant



● Truth Table

Input		Output
REN	**PAD**	**C**
x	1	1
x	0	0
0	pull-up	1
1	z	x

● Cell Information

Cell Name	No.Pad Req.	Power(µ W/MHz)
PICUW	**1**	**887.2**

● Pin Capacitance (pF)

Cell Name	C	PAD
PICUW		

PICUW

Input Pad with Controllable Pull-up , 5V-Tolerant

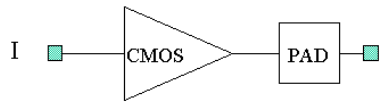
● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PICUW	PAD->C (fall)	0.2882	0.2914	0.298	0.311	0.2317*Cload+0.2890
PICUW	PAD->C (rise)	0.3434	0.3458	0.3513	0.3598	0.1559*Cload+0.3446

POxW

CMOS OUTPUT Only PAD , Tolerant



● Truth Table

Input	Output
I	Pad
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PO2W	1	71.81
PO4W	1	87.25
PO8W	1	92.37
PO12W	1	90.65
PO16W	1	101.2
PO24W	1	118.5

● Pin Capacitance (pF)

Cell Name	C	PAD
PO2W		
PO4W		
PO8W		

POxW

CMOS OUTPUT Only PAD , Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO2W	I->PAD (fall)	2.971	6.601	10.2	23.57	0.1789*Cload+1.2196
PO2W	I->PAD (rise)	2.914	6.598	10.23	23.76	0.1812*Cload+1.136

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO4W	I->PAD (fall)	1.814	3.622	5.419	12.12	0.0895*Cload+0.9331
PO4W	I->PAD (rise)	1.725	3.577	5.406	12.2	0.0910*Cload+0.8357

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO8W	I->PAD (fall)	1.284	2.193	3.089	6.44	0.0448*Cload+0.8435
PO8W	I->PAD (rise)	1.219	2.151	3.07	6.482	0.0457*Cload+0.7741

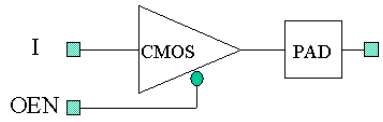
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO12W	I->PAD (fall)	1.129	1.737	2.336	4.568	0.0298*Cload+0.8407
PO12W	I->PAD (rise)	1.079	1.712	2.327	4.607	0.0306*Cload+0.7865

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO16W	I->PAD (fall)	1.069	1.526	1.976	3.65	0.0224*Cload+0.8512
PO16W	I->PAD (rise)	1.03	1.52	1.986	3.699	0.0231*Cload+0.8171

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PO24W	I->PAD (fall)	1.13	1.449	1.751	2.869	0.0151*Cload+0.9881
PO24W	I->PAD (rise)	1.092	1.451	1.772	2.923	0.0158*Cload+0.9602

POTxW

CMOS 3-STATE OUTPUT PAD, 5V-Tolerant



● Truth Table

Input		Output
OEN	I	PAD
1	x	Z
0	0	0
0	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)	Drive Capability(mA)
POT2W	1	72.52	
POT4W	1	88.06	
POT8W	1	91.44	
POT12W	1	98.42	
POT16W	1	99.07	
POT24W	1	115.6	

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
POT2W				
POT4W				
POT8W				
POT12W				
POT16W				

POTxW

CMOS 3-STATE OUTPUT PAD, 5V-Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25℃, typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT2W	I->PAD (fall)	2.971	6.601	10.2	23.57	0.1789*Cload+1.2196
POT2W	I->PAD (rise)	2.915	6.599	10.23	23.76	0.1812*Cload+1.1365
POT2W	OEN->PAD (fall)	2.807	6.437	10.03	23.4	0.1789*Cload+1.0526
POT2W	OEN->PAD (rise)	2.938	6.593	10.21	23.74	0.1808*Cload+1.1522

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT4W	I->PAD (fall)	1.814	3.622	5.419	12.12	0.0895*Cload+0.9331
POT4W	I->PAD (rise)	1.729	3.582	5.411	12.2	0.0909*Cload+0.8446
POT4W	OEN->PAD (fall)	1.719	3.527	5.324	12.03	0.0896*Cload+0.8340
POT4W	OEN->PAD (rise)	1.759	3.597	5.416	12.19	0.0906*Cload+0.8707

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT8W	I->PAD (fall)	1.284	2.193	3.089	6.44	0.0448*Cload+0.8435
POT8W	I->PAD (rise)	1.22	2.152	3.071	6.483	0.0457*Cload+0.7751
POT8W	OEN->PAD (fall)	1.236	2.14	3.037	6.387	0.0447*Cload+0.7973

POT8W	OEN->PAD (rise)	1.247	2.174	3.089	6.489	0.0455*Cload+0.8041

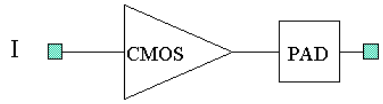
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT12W	I->PAD (fall)	1.129	1.737	2.336	4.568	0.0298*Cload+0.8407
POT12W	I->PAD (rise)	1.08	1.713	2.328	4.608	0.0306*Cload+0.7875
POT12W	OEN->PAD (fall)	1.095	1.698	2.296	4.528	0.0298*Cload+0.8025
POT12W	OEN->PAD (rise)	1.101	1.731	2.343	4.616	0.0305*Cload+0.8083

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT16W	I->PAD (fall)	1.069	1.526	1.976	3.65	0.0224*Cload+0.8512
POT16W	I->PAD (rise)	1.031	1.521	1.987	3.701	0.0232*Cload+0.813
POT16W	OEN->PAD (fall)	1.04	1.494	1.943	3.616	0.0223*Cload+0.8246
POT16W	OEN->PAD (rise)	1.05	1.536	1.999	3.708	0.0231*Cload+0.8316

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POT24W	I->PAD (fall)	1.13	1.449	1.751	2.869	0.0151*Cload+0.9881
POT24W	I->PAD (rise)	1.092	1.451	1.771	2.922	0.0158*Cload+0.9597
POT24W	OEN->PAD (fall)	1.107	1.424	1.726	2.842	0.0150*Cload+0.9685
POT24W	OEN->PAD (rise)	1.097	1.454	1.772	2.921	0.0158*Cload+0.9617

POLxW

CMOS OUTPUT Only PAD with LIMITED SLEW RATE , Tolerant



● Truth Table

Input	Output
I	Pad
1	1
0	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
POL8W	1	83.95
POL12W	1	95.45
POL16W	1	106.6
POL24W	1	124.2

● Pin Capacitance (pF)

Cell Name	C	PAD
POL8W		
POL12W		
POL16W		

POLxW

CMOS OUTPUT Only PAD with LIMITED SLEW RATE , Tolerant

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POL8W	I->PAD (fall)	1.464	2.373	3.27	6.62	0.0448*Cload+1.0237
POL8W	I->PAD (rise)	1.413	2.346	3.266	6.678	0.0457*Cload+0.9693

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POL12W	I->PAD (fall)	1.214	1.824	2.422	4.655	0.0299*Cload+0.9216
POL12W	I->PAD (rise)	1.162	1.796	2.411	4.691	0.0306*Cload+0.8702

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POL16W	I->PAD (fall)	1.615	2.131	2.597	4.28	0.0231*Cload+1.4141
POL16W	I->PAD (rise)	1.547	2.071	2.545	4.264	0.0236*Cload+1.3382

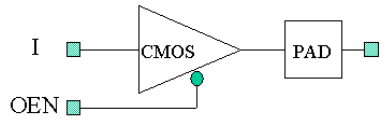
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POL24W	I->PAD (fall)	1.574	1.972	2.305	3.452	0.0162*Cload+1.455

POL24W	I->PAD (rise)	1.531	1.935	2.273	3.44 0.0165*Cload+1.4078

POTLxW

POTLxW

CMOS 3-STATE OUTPUT PAD, with LIMITED SLEW RATE , 5V-Tolerant



● Truth Table

Input		Output
OEN	**I**	**PAD**
1	x	Z
0	0	0
0	1	1

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)	Drive Capability(mA)
POTL8W	**1**	**85.69**	
POTL12W	**1**	**95.90**	
POTL16W	**1**	**111.5**	
POTL24W	**1**	**128.2**	

● Pin Capacitance (pF)

Cell Name	C	I	OEN	PAD
POTL8W				

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25℃, typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POTL8W	I->PAD (fall)	1.464	2.373	3.27	6.62	0.0448*Cload+1.0237
POTL8W	I->PAD (rise)	1.414	2.348	3.267	6.679	0.0457*Cload+0.9706
POTL8W	OEN->PAD (fall)	1.415	2.323	3.219	6.569	0.0448*Cload+0.9735
POTL8W	OEN->PAD (rise)	1.428	2.358	3.273	6.674	0.0455*Cload+0.9876

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POTL12W	I->PAD (fall)	1.214	1.824	2.422	4.655	0.0299*Cload+0.9216
POTL12W	I->PAD (rise)	1.163	1.797	2.412	4.692	0.0306*Cload+0.8712
POTL12W	OEN->PAD (fall)	1.178	1.785	2.382	4.614	0.0298*Cload+0.888
POTL12W	OEN->PAD (rise)	1.179	1.809	2.423	4.696	0.0305*Cload+0.8873

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POTL16W	I->PAD (fall)	1.615	2.131	2.597	4.28	0.0231*Cload+1.4141
POTL16W	I->PAD (rise)	1.548	2.072	2.546	4.265	0.0236*Cload+1.3392
POTL16W	OEN->PAD (fall)	1.572	2.092	2.558	4.241	0.0231*Cload+1.3741
POTL16W	OEN->PAD (rise)	1.535	2.06	2.533	4.248	0.0235*Cload+1.3308

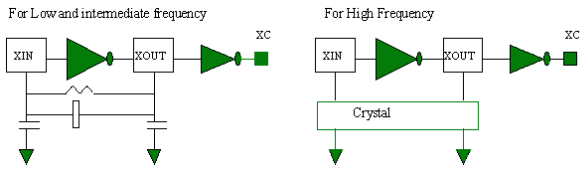
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
POTL24W	I->PAD (fall)	1.574	1.972	2.305	3.452	0.0162*Cload+1.455
POTL24W	I->PAD (rise)	1.533	1.936	2.275	3.441	0.0165*Cload+1.4093

POTL24W	OEN->PAD (fall)	1.546	1.949	2.282	3.429 0.0163*Cload+1.4253
POTL24W	OEN->PAD (rise)	1.507	1.912	2.251	3.416 0.0165*Cload+1.3846

PXxW

PXxW

Crystal Oscillator



● Truth Table

Input	Output	
XIN	**XOUT**	**XC**
1	0	1
0	1	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PX1W	**1**	**41.36**
PX2W	**1**	**49.38**
PX3W	**1**	**59.12**

● Pin Capacitance (pF)

Cell Name	XC	XIN	XOUT
PX1W			
PX1W			
PX1W			

PXx

Crystal Oscillator

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PX1W	XIN->XOUT (fall)	0.5512	1.199	1.843	4.254	0.0321*Cload+0.2364
PX1W	XIN->XOUT (rise)	0.5512	1.199	1.843	4.254	0.0321*Cload+0.2364
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PX2W	XIN->XOUT (fall)	0.515	1.011	1.495	3.304	0.0242*Cload+0.2805
PX2W	XIN->XOUT (rise)	0.515	1.011	1.495	3.304	0.0242*Cload+0.2805
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PX3W	XIN->XOUT (fall)	0.5081	0.9193	1.31	2.76	0.0195*Cload+0.3262
PX3W	XIN->XOUT (rise)	0.5081	0.9193	1.31	2.76	0.0195*Cload+0.3262

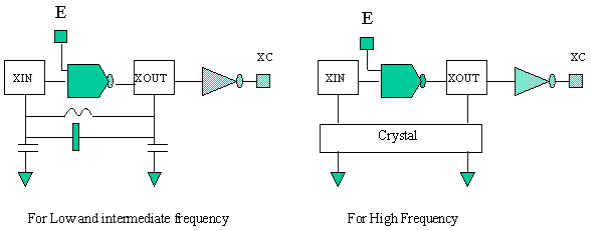
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PX1W	XIN->XC (fall)	0.478	0.4792	0.4808	0.4826	0.0429*Cload+0.4786
PX1W	XIN->XC (rise)	0.5041	0.506	0.5059	0.5103	0.0901*Cload+0.5034
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PX2W	XIN->XC (fall)	0.5011	0.5018	0.5051	0.509	0.0658*Cload+0.5019

PX2W	XIN->XC (rise)	0.5308	0.5298	0.5319	0.5348	0.0271*Cload+0.5308
cell	delay_path	Standard Load				Performance Equation
		2	4	8	16	
PX3W	XIN->XC (fall)	0.535	0.5357	0.5383	0.5375	0.5366-0.001*Cload
PX3W	XIN->XC (rise)	0.5633	0.5642	0.5712	0.5712	0.0128*Cload+0.5670

PXWExW

PXWExW

Crystal Oscillator with HIGH ENABLE



● Truth Table

Input		Output	
E	**XIN**	**XOUT**	**XC**
1	1	0	1
1	0	1	0
0	1	1	0
0	0	1	0

● Cell Information

Cell Name	No.Pad Req.	Power(μ W/MHz)
PXWE1W	**1**	**52.63**
PXWE2W	**1**	**60.76**

● Pin Capacitance (pF)

Cell Name	XC	XIN	XOUT
PXWE1W			
PXWE2W			
PXWE3W			

PXWEXW

Crystal Oscillator with HIGH ENABLE

● Propagation Delay(ns)

VDD_IO=3.3V, VDD_CORE=1.8V, temperature=25 ℃ , typical process, standard load=0.00699 pf, input slew time=0.06ns (measured from 10% to 90% transition)

cell	delay_path	Standard Load			Performance Equation
		2	4	8	16
PXWE1W	E->XC (rise)	0.5999	0.6017	0.6028	0.6043 0.0472*Cload+0.6005
PXWE1W	E->XC (fall)	0.8411	0.8433	0.8456	0.85 0.0944*Cload+0.8417
PXWE1W	XIN->XC (rise)	0.4833	0.4843	0.488	0.4909 0.0557*Cload+0.4846
PXWE1W	XIN->XC (fall)	0.5578	0.5597	0.563	0.5685 0.1058*Cload+0.5585
cell	delay_path	Standard Load			Performance Equation
		2	4	8	16
PXWE2W	E->XC (rise)	0.6236	0.6261	0.6281	0.6314 0.0829*Cload+0.6244
PXWE2W	E->XC (fall)	0.8779	0.8795	0.881	0.8839 0.0643*Cload+0.8783
PXWE2W	XIN->XC (rise)	0.5214	0.52	0.5218	0.5222 0.5218-0.014*Cload
PXWE2W	XIN->XC (fall)	0.5988	0.5996	0.6016	0.6028 0.0286*Cload+0.5997
cell	delay_path	Standard Load			Performance Equation
		2	4	8	16
PXWE3W	E->XC (rise)	0.6608	0.6615	0.6636	0.6654 0.0357*Cload+0.6615
PXWE3W	E->XC (fall)	0.9302	0.931	0.9296	0.9328 0.0572*Cload+0.9289
PXWE3W	XIN->XC (rise)	0.5549	0.5556	0.5587	0.5598 0.0257*Cload+0.5563
PXWE3W	XIN->XC (fall)	0.6487	0.6495	0.6509	0.6536 0.0500*Cload+0.6489

cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PXWE1W	E->XOUT (rise)	1.033	1.998	2.963	6.578	0.0482*Cload+0.5522
PXWE1W	E->XOUT (fall)	0.673	1.385	2.096	4.762	0.0355*Cload+0.3208
PXWE1W	XIN->XOUT (rise)	0.7645	1.732	2.697	6.313	0.0482*Cload+0.2858
PXWE1W	XIN->XOUT (fall)	0.7645	1.732	2.697	6.313	0.0482*Cload+0.2858
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PXWE2W	E->XOUT (rise)	0.926	1.568	2.21	4.62	0.0321*Cload+0.6056
PXWE2W	E->XOUT (fall)	0.615	1.123	1.631	3.535	0.0253*Cload+0.3661
PXWE2W	XIN->XOUT (rise)	0.6648	1.317	1.961	4.372	0.0322*Cload+0.3479
PXWE2W	XIN->XOUT (fall)	0.6648	1.317	1.961	4.372	0.0322*Cload+0.3479
cell	delay_path	Sample Loads(pf)				Performance Equation
		10	30	50	125	
PXWE3W	E->XOUT (rise)	0.9081	1.387	1.868	3.675	0.0240*Cload+0.6695
PXWE3W	E->XOUT (fall)	0.6043	1.001	1.395	2.877	0.0197*Cload+0.4104
PXWE3W	XIN->XOUT (rise)	0.6465	1.15	1.635	3.446	0.0243*Cload+0.4132
PXWE3W	XIN->XOUT (fall)	0.6465	1.15	1.635	3.446	0.0243*Cload+0.4132

PVDD1W

Digital Vdd power pad for I/O pre-driver & core (1.8V)

● Cell Information

Cell Name	No. Pad Req.
PVDD1W	1

PVDD2W

Digital Vdd power pad for I/O post-driver (3.3V)

● Cell Information

Cell Name	No. Pad Req.
PVDD2W	1

PVSS1W

Digital Vss ground pad for I/O pre-driver & core (1.8V)

● Cell Information

Cell Name	No. Pad Req.	Power(μ W/MHz)
PVSS1W	1	

PVSS2W

Digital Vss ground pad for I/O post-driver (3.3V)

● Cell Information

Cell Name	No. Pad Req.	Power(μ W/MHz)
PVSS2W	1	

PVSS3W

Digital Vss ground pad for ALL (I/O pre-driver, post-driver & core)

● Cell Information

Cell Name	No. Pad Req.
PVSS3W	1

Appendix A (Maximum Allowable Current for Digital Power and Ground Cells)

The following table lists the maximum allowable current for the *SP018W* I/O Digital power/ground cells including pad. The maximum allowable current for the different metal layers is provided. The power/ground cells will limit the maximum safety current for metal electro-migration consideration (EM).

Maximum Allowable Current Of Digital I/O Power/Ground Cells

	PVDD1W	PVDD2W	PVSS1W	PVSS2W	PVSS3W
Metal 4 tape-out	84mA	82mA	84mA	160mA	160mA
Metal 5 tape-out	84mA	82mA	84mA	208mA	208mA
Metal 6 tape-out	84mA	82mA	84mA	256mA	256mA

	PVDD1W	PVDD2W	PVSS1W	PVSS2W	PVSS3W
Metal layer of I/O that connect to core circuit	Metal 1-6	/	Metal 1-2	/	Metal 1-2

Please notice the maximum allowable current in table above is corresponding to I/O power/ground cells only. The amount of current that can be provided to the core logic is related to the number of metal layer that interconnect the I/O and core logic. For an example, PVSS1W use Metal 1 and 2 to connect with the core circuit.

Appendix B (Maximum Allowable Current for Analog Power and Ground Cells)

Maximum Allowable Current Of Analog I/O Power/Ground Cells

Analog I/O Cell	Metal 4 Tapeout	Metal 5 Tapeout	Metal 6 Tapeout	Metal layer of I/O that connect to core circuit
PANA1APW	84mA	84mA	84mA	Metal 1-2
PANA1AP1W	84mA	84mA	84mA	Metal 1-2
PANA2APW	17mA	17mA	17mA	Metal 2
PANA2AP1W	17mA	17mA	17mA	Metal 2
PVDD1APW	84mA	84mA	84mA	Metal 1-2
PVDD1AP1W	84mA	84mA	84mA	Metal 1-2
PVDD2APW	70mA	70mA	70mA	/
PVDD3APW	70mA	70mA	70mA	Metal 1-6
PVDD4APW	84mA	84mA	84mA	/
PVDD5APW	70mA	70mA	70mA	/
PVSS1APW	84mA	84mA	84mA	Metal 1-2
PVSS1AP1W	84mA	84mA	84mA	Metal 1-2
PVSS2APW	160mA	208mA	256mA	/
PVSS3APW	160mA	208mA	256mA	Metal 1-2
PVSS4APW	84mA	84mA	84mA	/
PVSS5APW	160mA	208mA	256mA	/
PVDD1ANPW	84mA	84mA	84mA	Metal 1-2
PVSS1ANPW	84mA	84mA	84mA	Metal 1-2
PVDD1CAPW	84mA	84mA	84mA	Metal 1-2
PVDD1CAP1W	84mA	84mA	84mA	Metal 1-2
PVSS1CAPW	84mA	84mA	84mA	Metal 1-2
PVSS1CAP1W	84mA	84mA	84mA	Metal 1-2
PVDD3CAPW	70mA	70mA	70mA	Metal 1-6
PVSS3CAPW	160mA	208mA	256mA	Metal 1-2
PANA4APW	40mA	40mA	40mA	Metal 2-3
PANA3APW	40mA	40mA	40mA	Metal 2-3

Please notice the maximum allowable current in table above is corresponding to I/O power/ground cells only. The amount of current that can be provided to the core logic is related to the number of metal layer that interconnect the I/O and core logic. Please take notice that metal layer of PANA2APW and PANA2AP1W I/Os that connect to core logic is metal 2.