Realization of FPGA Based PID Controller for Speed Control of DC Motor Using Xilinx SysGen

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Abstract. PID controllers can be designed using analog and digital methods; digital PID controllers are most significantly used in the industries. FPGA based PID Controllers are preferred because of their improved settling time and are small in size, consume power efficiently and provide high speed of operation compared to software based PID controllers or microprocessor/microcontroller based PID controllers. The effort has been taken to implement the digital PID controller using FPGA device based on multiplier principle, which is implemented using MATLAB Simulink and system generator. The controller is designed for speed control of dc motor and implementation is accomplished on Xilinx Spartan 3 FPGA chip to achieve the settling time of 10 s this shows 5 s early settlement compared to basic PID controller. The resources consumption of the scheme is also presented.

Keywords: Proportional Integral Derivative (PID) · Field Programmable Gate Array (FPGA) device · System generator (SysGen)

1 Introduction

An industrial control system is divided in two areas a plant and a unit required to control the behavior of plant i.e. plant is the utility which is controlled by the controller [1]. There are various controllers available to control the plant like proportional, derivative and integral controller separately or in the combination, amongst them Proportional Integral Derivative controller is one of the most utilizable type of feedback controller which is used for controlling the dynamic plants [2]. The digital PID controller can be implemented using microprocessors, microcontrollers or programmable logic controllers (PLC), but the drawback of these systems is the speed of operation, as the more time is required to fetch, decode, execute the code. Wherein FPGA based systems poised to be simpler and they provide high processing speed and high reconfiguration level [2]. A FPGA deals with high clock frequency, accuracy and programmable features, has noteworthy returns compared with various types of controllers. Moreover, an FPGA-based system can process signals from different kinds of sensors and FPGA development boards are often equipped with high number of input pins and they are easily available

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at cheaper price. In the proposed FPGA-based system, Xilinx® XC3S400 FPGA works as the foundation of the system. The system is designed using Simulink and then hardware in realized in Xilinx by programming with Very-High-Speed Integrated Circuit Hardware Description Language (VHDL). Thus system achieve the better settling time by controlling the speed of dc motor wherein this is achieved by parallel, operations and architectural design of digital controllers [7].

The paper is focused on the design of FPGA based digital PID Controller with multipliers; the computations are performed using multipliers [1].

2 PID Controllers

The PID controller is combination of proportional, integral and derivative control. The design needs basic mathematical operations, based on the increase in complexity and this has been overcome to some extent by using the digital PID controller [2].

The general PID equation is given as:

$$u(t) = K\left(e(t) + \frac{1}{T_i}\int_0^t e(t)dt + T_d\frac{de(t)}{dt}\right) \tag{1}$$

Where,

e(t) = Error signal
u(t) = Command signal
K = Gain or proportional gain
T_i = Integration time or rise time
T_d = Derivative time.

System wherein the PID controller is operating as feedback element is shown in Fig. 1, where Proportional, integral and derivative controller works with feedback loop. The PID controller is defined by Eq. 1, in which e is the error signal which is sent to PID controller. The signal passed to system is combination of proportional, integral and derivative terms related to error signal.

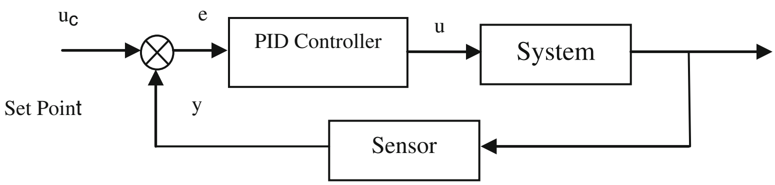

Fig. 1. PID based feedback control system

A proportional term helps to cut down the rise time, but it never get rid of the steady-state error, while an integral term eliminate the steady-state error, but it could show the worst transient response and a derivative term enhances the stability of the system, reduce the overshoot, and improves the transient response [3].

PID controller feedback control system implemented using Simulink is shown in Fig. 2.

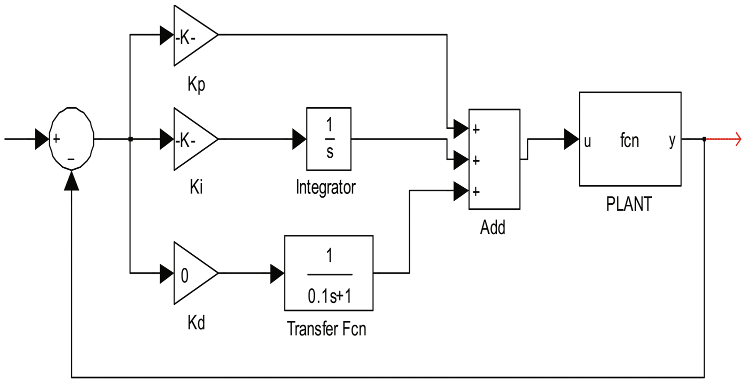

Fig. 2. PID controller with feedback using Simulink

Taking laplace transform of Eq. (1) we get

$$U(s) = \mathrm{K}\left(\mathrm{E(s)} + \frac{1}{\mathrm{sT_i}}\mathrm{E(s)} + \mathrm{sT_D E(s)}\right) \tag{2}$$

$$U(s) = \mathrm{KE(s)}\left(1 + \frac{1}{\mathrm{sT_i}} + \mathrm{sT_D}\right) \tag{3}$$

Where, if $K = K_P$, then $K_I = K_P/T_I$ and $K_D = K_P T_D$. Then the equation can be rewritten as [1]

$$U(s) = K_P\mathrm{E(S)} + \frac{\mathrm{K_I}}{\mathrm{S}}\mathrm{E(S)} + \mathrm{K_D SE(S)} \tag{4}$$

To take in the system by FPGA, the system is needed to be converted to discrete form this is achieved by transformation technique, and thus the continuous-time system is converted to discrete-time system [5],

$$D(z) = \frac{U(Z)}{E(Z)} = K_P + \mathrm{K_I}\frac{\mathrm{T_S}}{1 - \mathrm{Z}^{-1}} + \mathrm{K_D}\frac{1 - \mathrm{Z}^{-1}}{\mathrm{T_S}} \tag{5}$$

Where, T_s is the sampling time.

3 Plant Implementation

DC motors are usually very high-speed, revolving at several thousand revolutions per minute (rpm); they are simple to operate and their initial torque is large, because of which they are preferred for several traction operations for velocity control and in high speed control applications.

The dc motor has special characteristic to operate either on a.c. or d.c. supply based on different applications. The moment of inertia, damping, electromotive force, electric resistance, and electric inductance are the parameters considered for the control of dc motor, works as a plant (Table 1).

Table 1. DC motor parameters

Moment of inertia in the rotor	$J = 0.02\ kg{\cdot}m^2$
Damping (friction) of the mechanical system	$b = 0.15$ Nms
Electromotive force constant	$K = 0.011$ Nm/A
Electric resistance	$R = 1.2\ \Omega$
Electric inductance	$L = 0.6$ H

The input to the plant is armature voltage V in volts. Measured variables are the angular velocity of the shaft ω in radians per second and the shaft angle θ in radians [6]. Transfer function is for the dc motor is represented by Eq. 6.

$$\mathit{Transfer\ Function} = \frac{0.011}{0.012S^3 + 0.114S^2 + 0.1801S} \tag{6}$$

4 Design of Multiplier Based PID Controller

System generator is a tool for designing high performance DSP systems using FPGA. Figure 3 shows PID controller built using system generator toolbox. The PID controller is created according to the Eq. 7 [4] (Fig. 4).

$$U(s) = K_P e + K_I\left(I_{n-1} + edt\right) + K_D \frac{e - e_{n-1}}{dt} \tag{7}$$

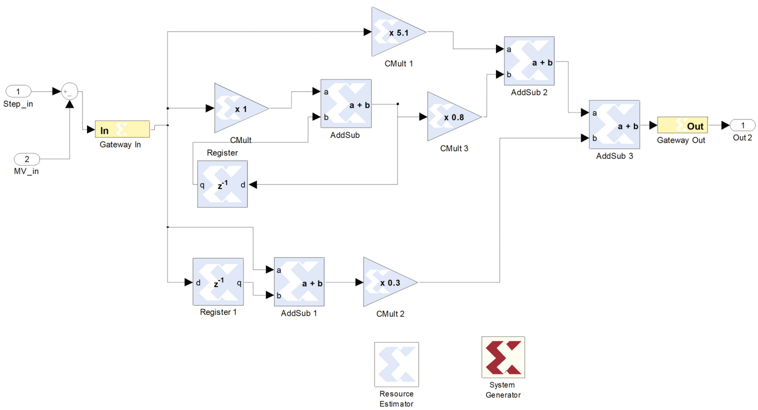

Fig. 3. Multiplier based PID controller

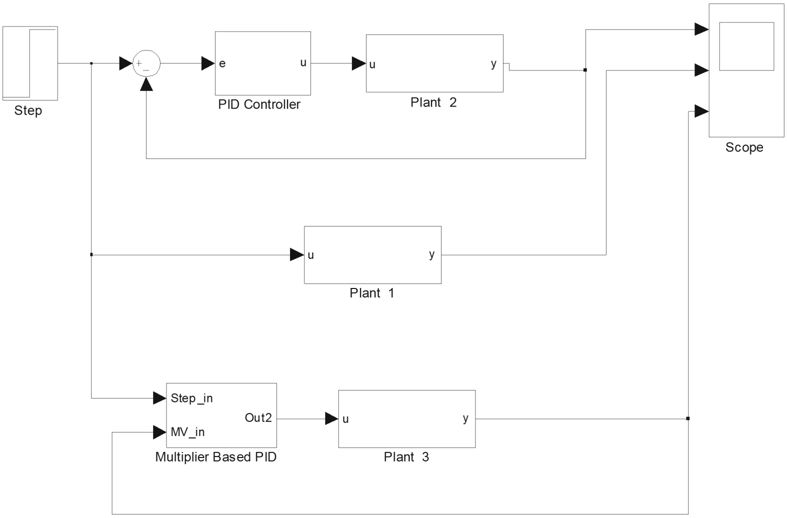

Fig. 4. Simulink implementation of various systems (basic PID controller, system without controller, multiplier based PID controller)

5 Results

The results of the model are presented in Fig. 5, where comparison between basic PID controller, system behaviour without PID Controller and multiplier based PID controller is presented. The graphical representation shows that Settling time of multiplier based PID controller is 5 s before the basic PID controller. Hence this design model will help to control the speed of dc motor efficiently.

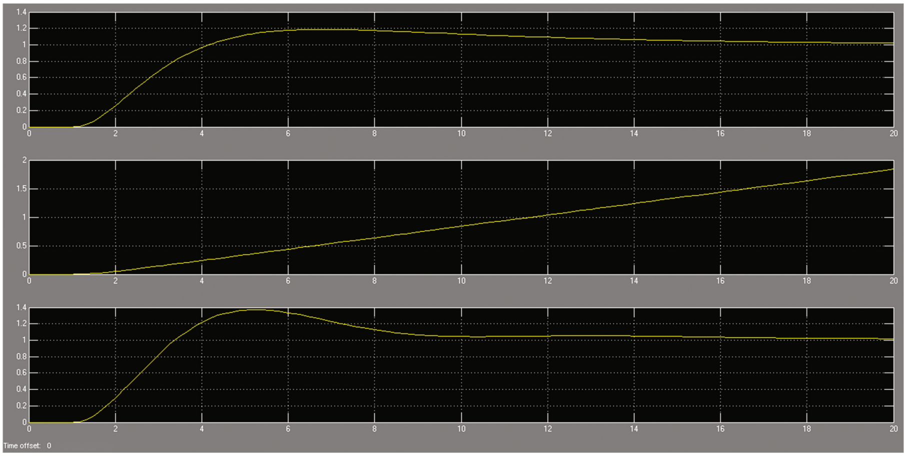

Fig. 5. Output comparison for various PID controllers

The designed Multiplier based PID controller is synthesized using Xilinx ISE 10.1. The target device used to implement the design is Spartan 3 XC3S400 FPGA. The summary of recourses utilized is presented in Table 2.

Design statistics: Minimum period: 5.031 ns (Maximum frequency: 198.768 MHz).

Table 2. Device utilization summary

	Used	Available	Utilization
Logic utilization			
Number of slice flip flops	40	7,168	1%
Number of 4 input LUTs	587	7,168	8%
Logic distribution			
Number of occupied Slices	328	3,584	9%
Number of slices containing only related logic	328	328	100%
Number of slices containing unrelated logic	0	328	0%
Total number of 4 input LUTs	624	7,168	8%
Number used as logic	587		
Number used as a route-thru	37		
Number of bonded IOBs	68	141	48%
Number of BUFGMUXs	1	8	12%
Number of RPM macros	4		

6 Conclusion

The current model achieves improved accuracy, compactness with time constraints by the effective use of FPGA and hardware utilization. The improved performance of multiplier based PID controller gives decrease in settling time as compared to the basic PID controller by 5 s. The future work implies to achieve effective resource utilization, less power consumption and increase in speed of operation with the use of DA based or multiplierless PID controller.

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